

Altera FPGA Dynamic Probe

[Online Help](#)



Agilent Technologies

Notices

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Using the Altera FPGA Dynamic Probe

When the Altera LAI (Logic Analyzer Interface) core has been inserted into an FPGA, the FPGA dynamic probe lets a logic analyzer capture data on signals internal to the FPGA.

The FPGA dynamic probe lets you change probe points without recompiling or affecting the timing of the design, and it lets you import internal signal names from your FPGA design tool.

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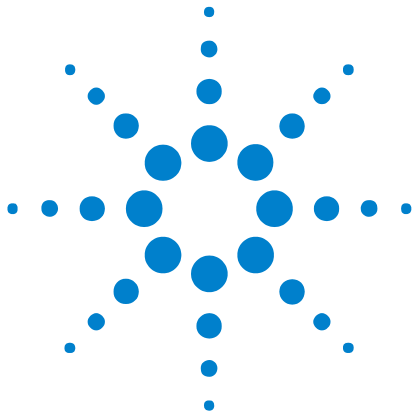
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1 Overview

The FPGA dynamic probe lets you:

- *View internal activity.*

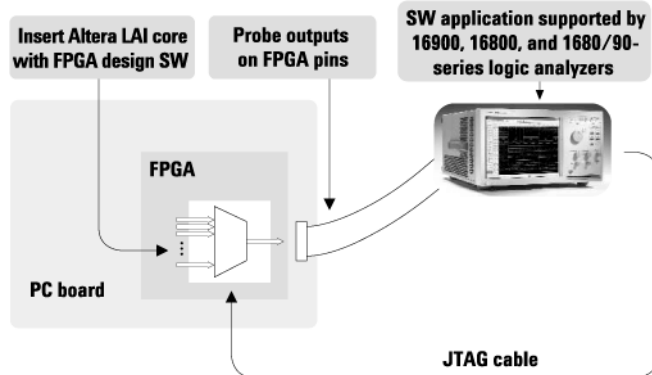
With a logic analyzer, you are normally limited to measuring signals at the periphery of the FPGA. With the FPGA dynamic probe, you can now access signals internal to the FPGA. You can measure multiple internal signals for each external pin dedicated to debug, unlocking visibility into your design that you never had before.

- *Make multiple measurements in seconds.*

Moving probe points internal to an FPGA used to be time consuming. Now, in less than a second you can easily measure a different set of internal signals – without design changes – and FPGA timing stays constant when you select new sets of internal signals for probing.

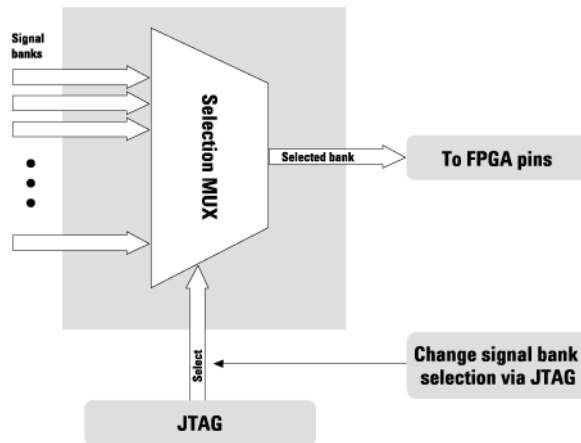
- *Leverage the work you did in your design environment.*

The FPGA dynamic probe is the industry's first tool that maps internal signal names from your FPGA design tool to your logic analyzer. Eliminate unintentional mistakes and save hours of time with this automatic setup of signal and bus names on your logic analyzer.

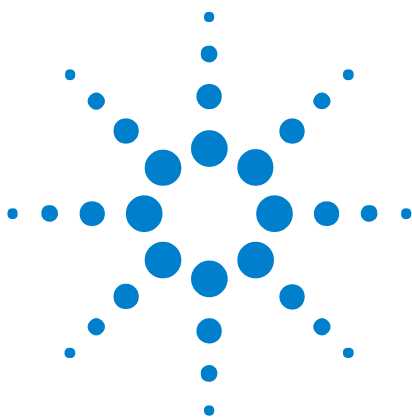


Create a time-saving FPGA measurement system. Insert an Altera LAI (Logic Analyzer Interface) core into your FPGA design. With the application running on your logic analyzer via JTAG, you control which group of internal signals to measure.

1 Overview



The Altera LAI core provides a multiplexer for selecting the signals that are output to FPGA debug pins. Core parameters determine the number of signals per bank and the number of banks.



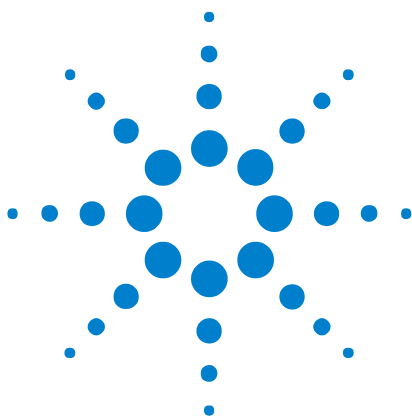
2 Probing FPGA Debug Pins

The supported mechanisms for probing the FPGA debug pins with a logic analyzer are: soft touch (34-channel or 17 channel), Mictor, Samtec, and flying lead probes.

For more information on probing, see "Probing the Device Under Test" (in the online help).



2 Probing FPGA Debug Pins



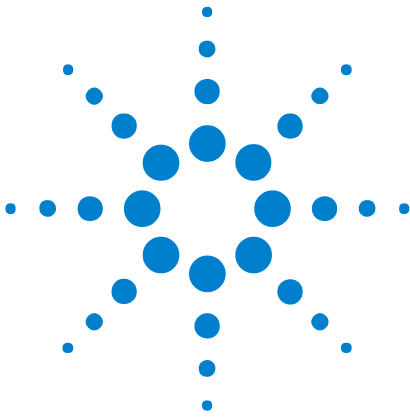
3 Installing and Licensing the FPGA Dynamic Probe

Before you can use the Agilent B4656A FPGA dynamic probe for Altera FPGAs, you must install and license the software:

- 1 Install the FPGA dynamic probe software from the download web page at:
["http://www.agilent.com/find/la-sw-download"](http://www.agilent.com/find/la-sw-download)
- 2 Follow the instructions on your entitlement certificate to redeem and install the FPGA dynamic probe license.



3 Installing and Licensing the FPGA Dynamic Probe



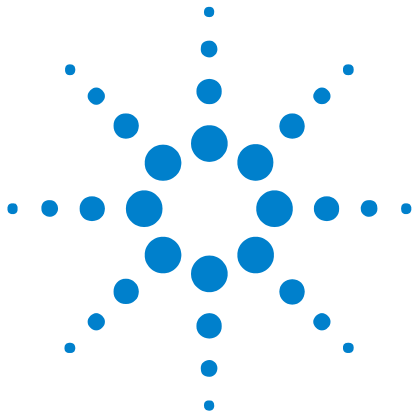
4 FPGA Design Steps

Altera LAI cores are inserted into FPGAs using Altera's Quartus II design software. For more information, see Altera's web site at "www.altera.com".

See Also • Preparation Steps (see [page 17](#))



4 FPGA Design Steps



5 Preparation Steps

Before you can use the FPGA dynamic probe software with the *Agilent Logic Analyzer* application, you must take these preparation steps:

- 1 Install the JTAG cable programmer software (see [page 18](#))
- 2 Set up the JTAG cable using the programmer software (see [page 19](#))

See Also • [Measurement Steps](#) (see [page 27](#))



Step 1. Install the JTAG cable programmer software

Before you can use the FPGA dynamic probe for Altera FPGAs, you must download and install the free Altera Quartus II Programmer software on the same logic analysis system or PC that the *Agilent Logic Analyzer* application runs on.

NOTE

The PC that has the JTAG cable connection to the device under test does not have to be the logic analysis system or PC that the *Agilent Logic Analyzer* application runs on. In this case, the logic analysis system communicates via LAN with the system that has the JTAG server (and cable connection to the DUT).

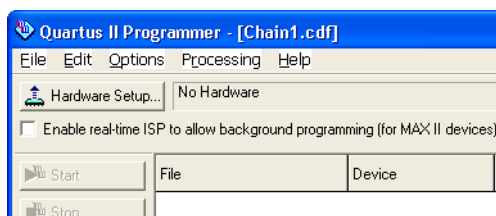
- 1 Download the Altera Quartus II Programmer software from:
"https://www.altera.com/support/software/download/programming/quartus2/dnl-quartus2_programmer.jsp"
- 2 Follow the installation instructions to install the software on the same logic analysis system or PC that the *Agilent Logic Analyzer* application runs on.
- 3 If the PC or logic analysis system that has the JTAG cable connection to the device under test is not the same computer that runs the *Agilent Logic Analyzer* application, and Quartus II design software is not already installed, install the Quartus II Programmer software there too.

- Next**
- Step 2. Set up the JTAG cable using the programmer software (see [page 19](#))

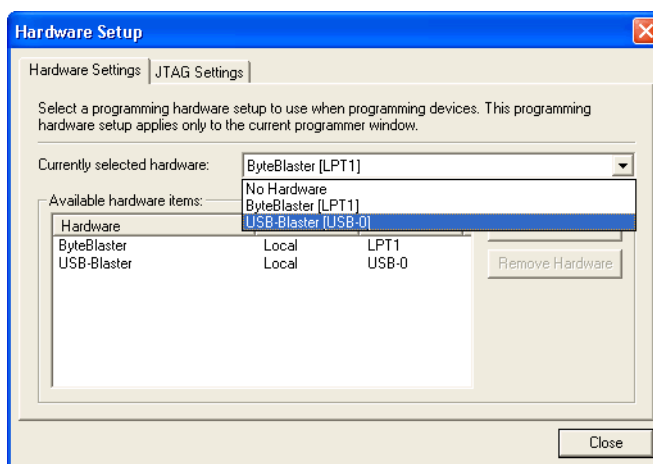
Step 2. Set up the JTAG cable using the programmer software

On the PC or logic analysis system that has the JTAG cable connection to the device under test:

- 1 If you are using the USB Blaster cable, driver files come with the Altera Quartus II Programmer software, but you must install them. See To install the USB Blaster device driver (see [page 20](#)).
- 2 Open the Altera Quartus II Programmer (or design) software and set up the JTAG cable connection:
 - a From the Windows Start menu, choose **All Programs>Altera>Quartus II 7.2 Programmer and SignalTap II>Quartus II 7.2 Programmer**.
 - b In the Quartus II Programmer window, click **Hardware Setup...**



- c In the Hardware Setup dialog, select the appropriate JTAG cable hardware.



You may have to click **Add Hardware...** to add the appropriate JTAG cable hardware.

- d After you have selected the appropriate JTAG cable hardware, click **Close** to close the Hardware Setup dialog.
 - e Choose **File>Exit** to close the Quartus II Programmer software.

If the PC or logic analysis system that has the JTAG cable connection to the device under test is not the same computer that will run the *Agilent Logic Analyzer* application, you must set up a JTAG server. See "[To set up a JTAG Server](#)" on page 21.

- Next**
- Step 3. Establish connection between analyzer and JTAG cable (see [page 28](#))

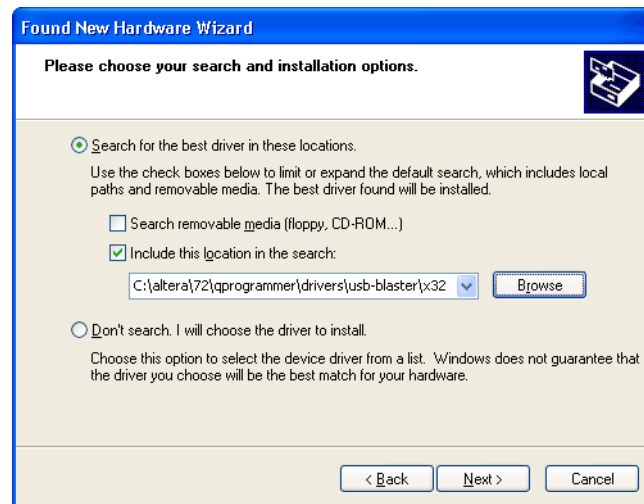
To install the USB Blaster device driver

On the PC or logic analysis system that has the JTAG cable connection to the device under test:

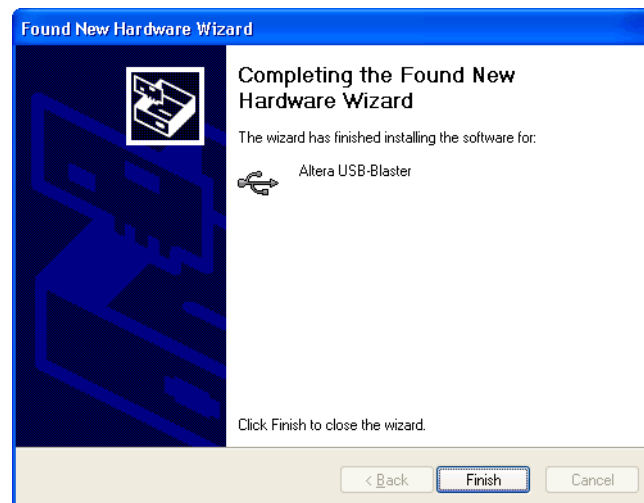
- 1 Connect the USB Blaster device to your computer.
- 2 In the Found New Hardware Wizard dialog, select **Install from a list or specific location**; then, click **Next >**.



- 3 On the next page of the wizard, specify the **drivers\usb-blaster\x32** (for a 32-bit operating system) or **drivers\usb-blaster\x64** (for a 64-bit operating system) location underneath the Quartus II Programmer install directory; then, click **Next >**.



- 4 When the wizard has finished installing the driver, click **Finish**.



For more information on installing the USB Blaster driver, see "<http://www.altera.com/support/software/drivers/usb-blaster/dri-usb-blaster-xp.html>" (or search for "USB Blaster driver" on the Altera web site).

To set up a JTAG Server

The Altera FPGA Dynamic Probe can connect to JTAG cables over a TCP/IP connection. This is useful when you want to remotely connect to a logic analysis system that also has the JTAG cable connection to the device under test. In this case, the *Agilent Logic Analyzer* application (and the Altera FPGA Dynamic Probe software), must communicate remotely with the logic analysis system as well as the JTAG cable server.

5 Preparation Steps

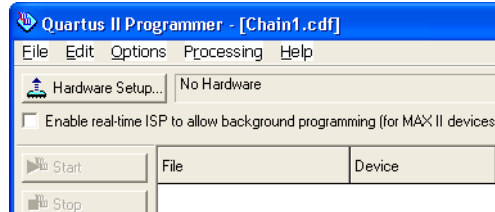
If your JTAG cable is connected between the device under test and the logic analysis system or PC that is running the *Agilent Logic Analyzer* application, you do not need to set up a JTAG server.

To set up the Altera Programmer software to allow client/server connections to a remote JTAG cable:

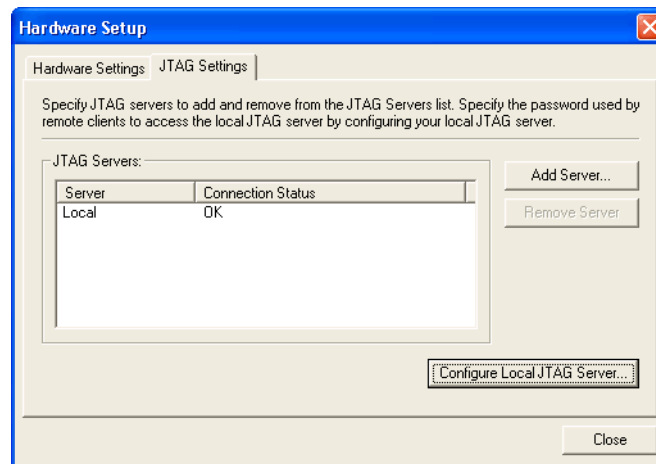
- 1 Make sure the Altera Quartus II Programmer software is installed on both:
 - The *client computer* where you will be running the *Agilent Logic Analyzer* application (the JTAG Client).
 - The *remote computer* (logic analysis system or PC) that is physically connected to the JTAG cable (the JTAG Server).

This should have already been done in "[Step 1. Install the JTAG cable programmer software](#)" on page 18.

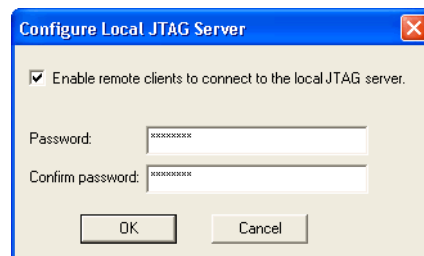
- 2 Set up the JTAG Server on the *remote computer*:
 - a Start the Quartus II Programmer application from the Windows Start menu by choosing **All Programs>Altera>Quartus II 7.2 Programmer and SignalTap II>Quartus II 7.2 Programmer**.
 - b In the Quartus II Programmer window, click **Hardware Setup...**



- c In the Hardware Setup dialog's JTAG Settings tab, click **Configure Local JTAG Server...**



- d In the Configure local JTAG Server dialog, check **Enable remote clients to connect to the local JTAG server**, enter a password, and confirm the password.



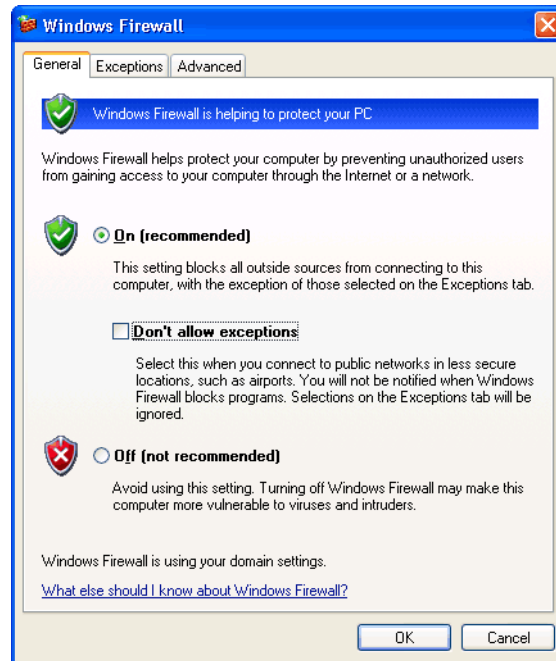
Record this password as you will need it later. Then, click **OK**.

- e Click **Close** to close the Hardware Setup dialog.
- f Choose **File>Exit** to close the Quartus II Programmer software.
- 3 If the *remote computer* is running firewall software, allow access to the JTAG Server through the firewall. If the remote computer is not running firewall software, you can skip this step and proceed to step 4.

For example, if the *remote computer* is running Windows Firewall:

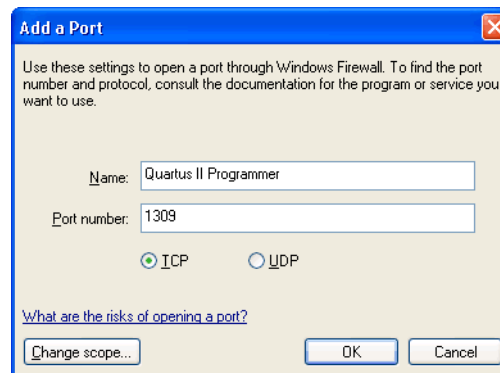
- a Make sure you are logged in as an administrator.
- b From the Windows Start menu, choose **Control Panel>Windows Firewall**.
- c In the Windows Firewall dialog's General tab, uncheck **Don't allow exceptions**.

5 Preparation Steps



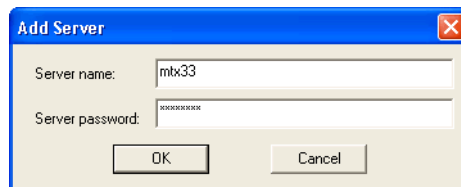
If the firewall is off, it may be that the computer is using different firewall software. In this case, you must enable access to the Quartus II Programmer port using the different firewall software.

- d In the Exceptions tab, click **Add Port...**
- e In the Add a Port dialog:
 - i Enter the **Name**: Quartus II Programmer.
 - ii Enter the **Port number**: 1309.
 - iii Select **TCP**.
 - iv Click **OK** to close the Add a Port dialog.



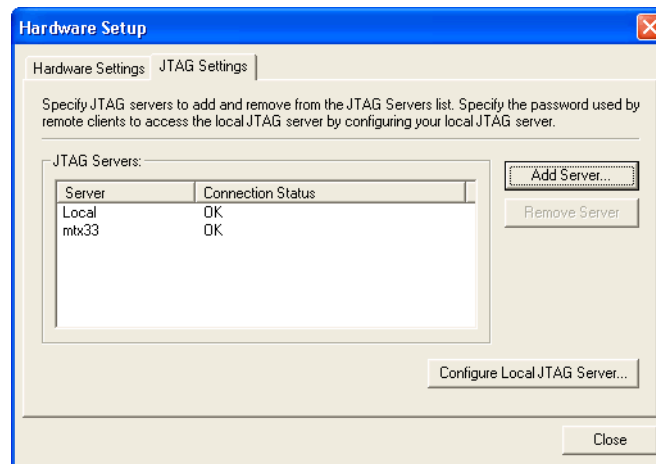
- e Click **OK** to close the Windows Firewall dialog.

- 4 Get the hostname of the *remote computer* (JTAG Server):
 - a From the Windows Start menu, choose **Control Panel>System**.
 - b Click the **Computer Name** tab.
 - c Write down the "Full computer name". This is the hostname of your remote JTAG server which you will need shortly.
 - d Click **OK**.
- 5 Set up the JTAG Client on the *client computer*:
 - a Start the Quartus II Programmer application from the Windows Start menu by choosing **All Programs>Altera>Quartus II 7.2 Programmer and SignalTap II>Quartus II 7.2 Programmer**.
 - b In the Quartus II Programmer window, click **Hardware Setup...**
 - c In the Hardware Setup dialog's JTAG Settings tab, click **Add Server...**
 - d In the Add Server dialog:
 - i Enter the full hostname of the remote JTAG Server you found in step 4.c as the **Server name**.
 - ii Enter the password you created in step 2.d as the **Server password**.
 - iii Click **OK**.



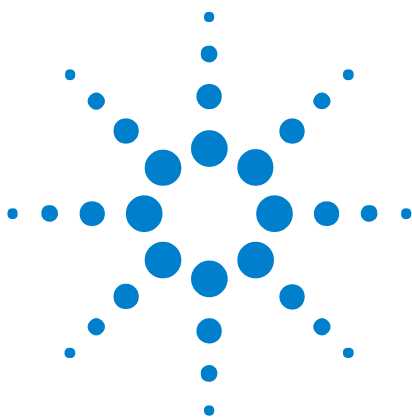
- d Verify that the Hardware Setup dialog shows a Connection Status of "OK". If not, then there is a problem with the networking. Re-verify your firewall settings and server-name/server-password settings.

5 Preparation Steps



- e Click **Close** to close the Hardware Setup dialog.
- f Choose **File>Exit** to close the Quartus II Programmer software.

Now, when you establish the connection between the analyzer and the JTAG cable (see "[Step 3. Establish connection between analyzer and JTAG cable](#)" on page 28), the remote JTAG cable will be listed in the Cable Connection dialog.



6 Measurement Steps

After you have completed the FPGA Design Steps (see [page 15](#)) and Preparation Steps (see [page 17](#)), you are ready to take these measurement steps in the *Agilent Logic Analyzer* application:

- 1 Establish connection between analyzer and JTAG cable (see [page 28](#))
- 2 Download configuration bits into FPGA (see [page 30](#))
- 3 Import signal names (see [page 31](#))
- 4 Map FPGA pins (see [page 35](#))
- 5 Make the measurement (see [page 39](#))

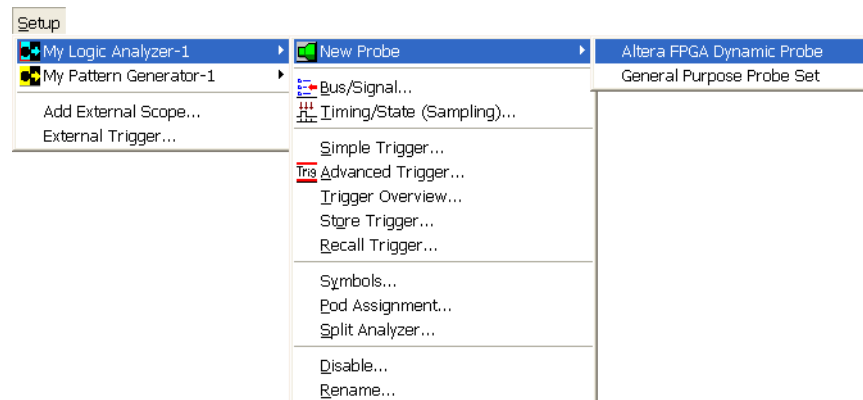


Step 3. Establish connection between analyzer and JTAG cable

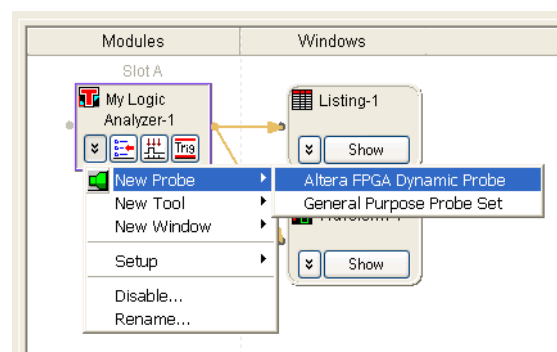
The FPGA dynamic probe application establishes a connection between the logic analyzer and a Xilinx cable. It also determines what devices are on the JTAG scan chain and lets you pick which one you wish to communicate.

To establish a connection between the logic analyzer and the Altera LAI core:

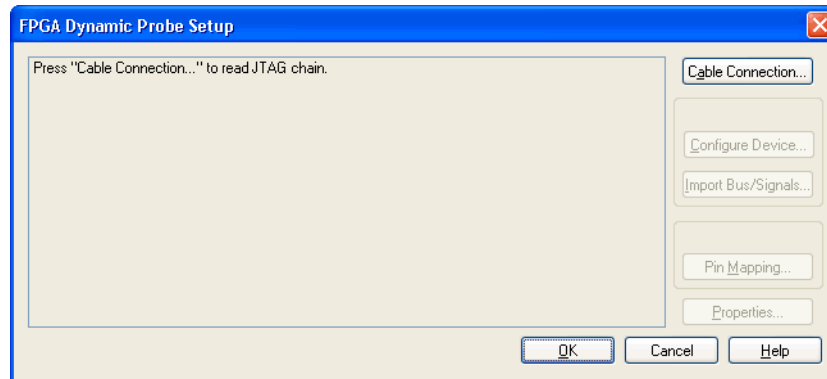
- 1 Add a new FPGA Dynamic Probe set by choosing **Setup>(Logic Analyzer Module)>New Probe>FPGA Dynamic Probe**.



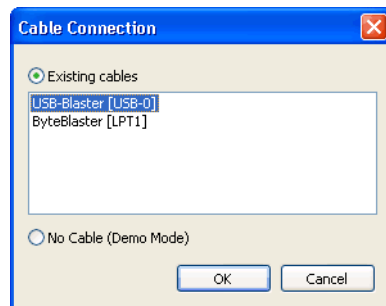
Or, in the Overview window, from a module's drop-down menu, choose **New Probe>FPGA Dynamic Probe**.



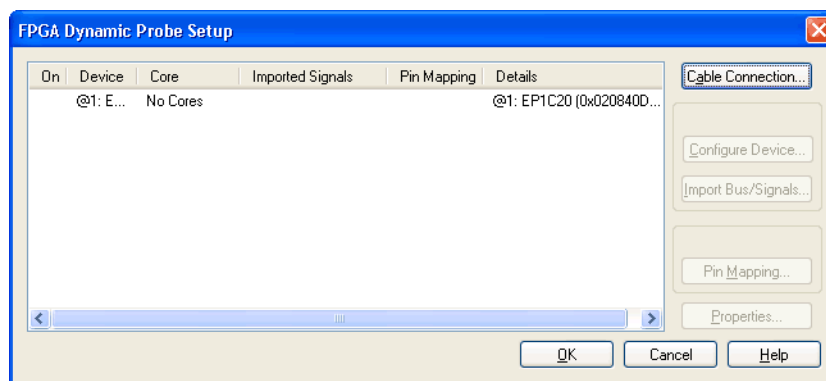
- 2 In the FPGA Dynamic Probe Setup dialog (see [page 50](#)), click **Cable Connection...**



- 3 In the Cable Connection dialog (see [page 51](#)), select the type of cable and, if necessary, specify any cable parameters; then, click **OK**.



When the connection has been established, you will see the devices on the JTAG chain, and you can select the desired device.

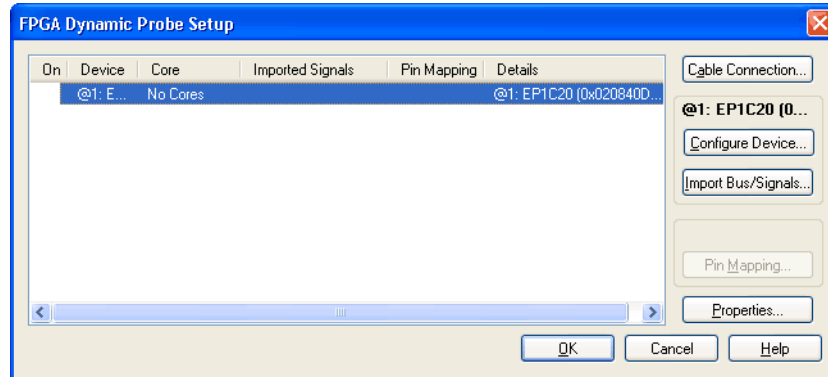


- Next** • Step 4. Download configuration bits into FPGA (see [page 30](#))

Step 4. Download configuration bits into FPGA

To download configuration bits into an FPGA:

- 1 In the FPGA Dynamic Probe Setup dialog (see [page 50](#)), select the FPGA device to which you wish to download configuration bits; then, click **Configure Device...**



- 2 In the Select FPGA Configuration File dialog (see [page 54](#)), select the FPGA configuration file; then, click **Open**.

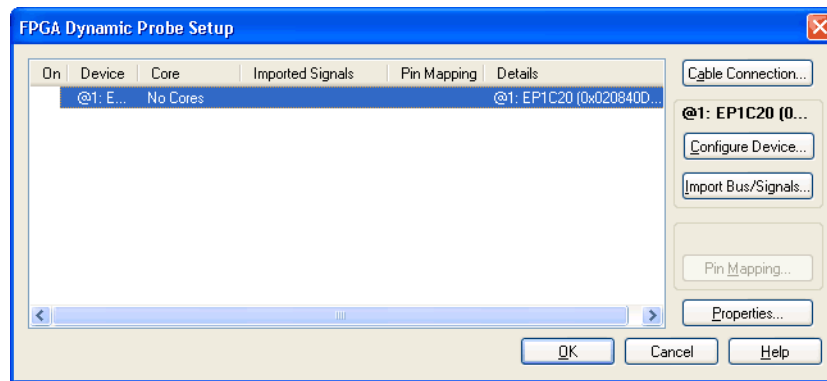
Next • Step 5. Import signal names (see [page 31](#))

Step 5. Import signal names

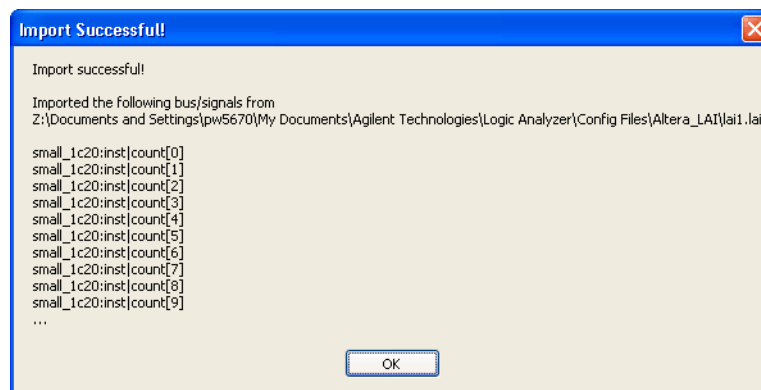
The FPGA dynamic probe can automatically set up bus/signal names in the logic analyzer by reading a .lai file produced by Altera's Quartus II LAI (Logic Analyzer Interface) design software.

To import bus/signal names:

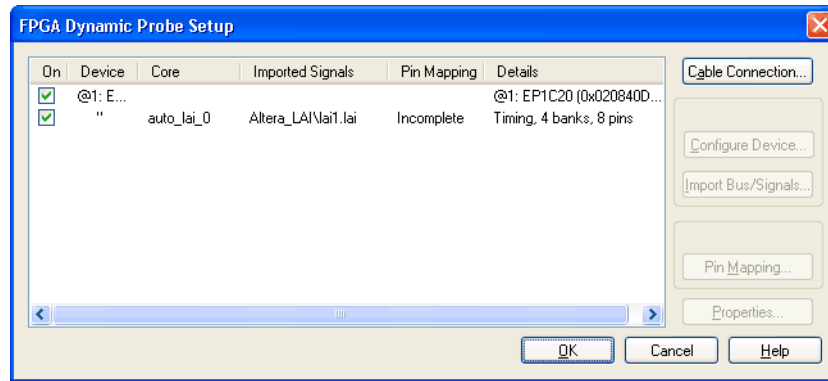
- 1 In the FPGA Dynamic Probe Setup dialog (see [page 50](#)), select the device whose bus/signal names you want to import; then, click **Import Bus/Signals....**



- 2 In the Select Signal Import File dialog (see [page 54](#)), select the signal import file; then, click **Open**.
- 3 In the import results dialog, view the bus/signal import information; then, click **OK**.



- 4 In the FPGA Dynamic Probe dialog, note that the defined cores now appear.



- See Also**
- To trim imported bus/signal names (see [page 32](#))
 - To rename imported bus/signal names (see [page 32](#))
 - To define additional FPGA bus/signal names (see [page 33](#))
- Next**
- Step 6. Map FPGA pins (see [page 35](#))

To trim imported bus/signal names

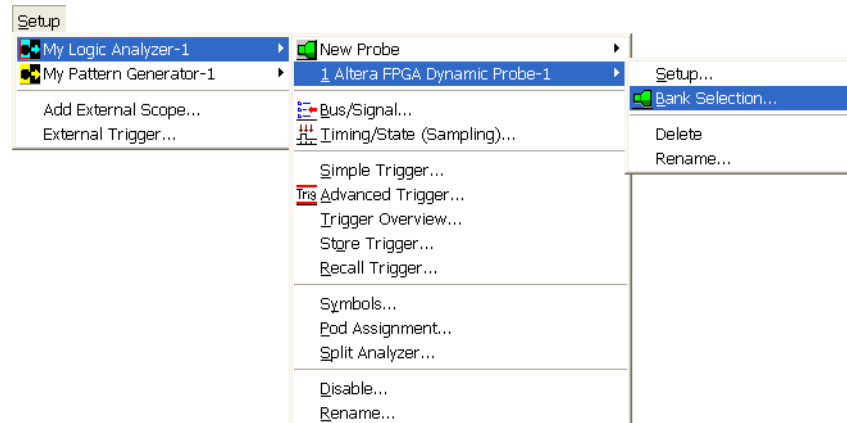
NOTE

Trimming bus/signal names after initial bank selection may require manual insertion of bus/signals in Waveform and Listing display windows. We recommend that you trim bus/signal names before changing the bank selection.

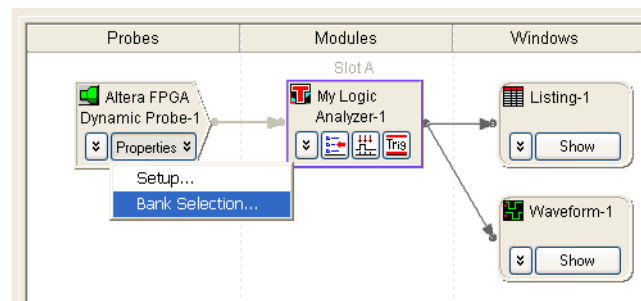
- 1 In the FPGA Dynamic Probe Bank Selection dialog (see [page 57](#)), click **Trim Bus/Signal Names...**
- 2 In the Trim Bus/Signal Names dialog (see [page 57](#)), specify the bus/signal name characters to trim; then, click **OK**.

To rename imported bus/signal names

- 1 Open the Buses/Signals setup tab (see "Defining Buses and Signals" (in the online help)).
- 2 In the "FPGA Probe" bus/signal name folder, rename the bus/signal (see "To rename a bus or signal" (in the online help)).
- 3 Reopen the FPGA Dynamic Probe dialog by choosing **Setup>(Logic Analyzer Module)>(FPGA Dynamic Probe Name)>Bank Selection...**



Or, in the Overview window, click the FPGA dynamic probe's **Properties** button; then, choose **Bank Selection...**

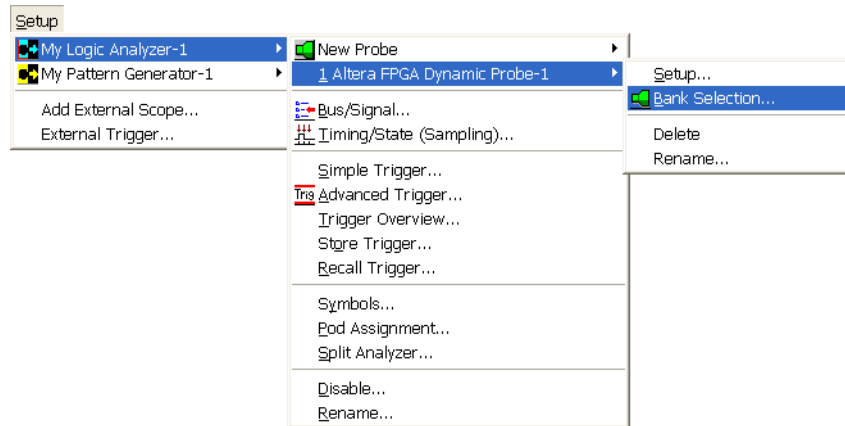


Note also that you can triple-click signal names in the FPGA Dynamic Probe dialog to rename them (without having to do global trimming).

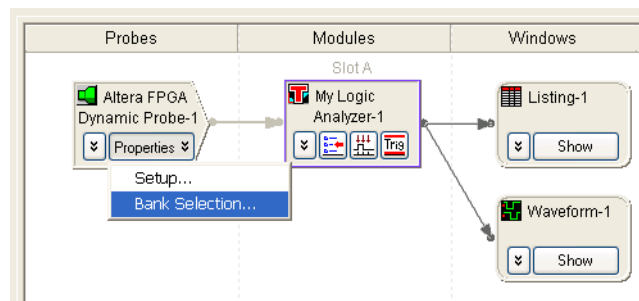
To define additional FPGA bus/signal names

- 1 Open the Buses/Signals setup tab (see "Defining Buses and Signals" (in the online help)).
- 2 In the "FPGA Probe" bus/signal name folder, add a new bus/signal (see "To add a new bus or signal" (in the online help)).
- 3 Assign channels to the new bus/signal name (see "To assign channels in the default bit order" (in the online help) or "To assign channels, selecting the bit order" (in the online help)).
- 4 Reopen the FPGA Dynamic Probe dialog by choosing **Setup>(Logic Analyzer Module)>(FPGA Dynamic Probe Name)>Bank Selection...**

6 Measurement Steps



Or, in the Overview window, click the FPGA dynamic probe's **Properties** button; then, choose **Bank Selection...**



Whenever buses/signals are added to the "FPGA Probe" folder, they are associated with a specific bank. If you select another bank, the added buses/signals do not appear.

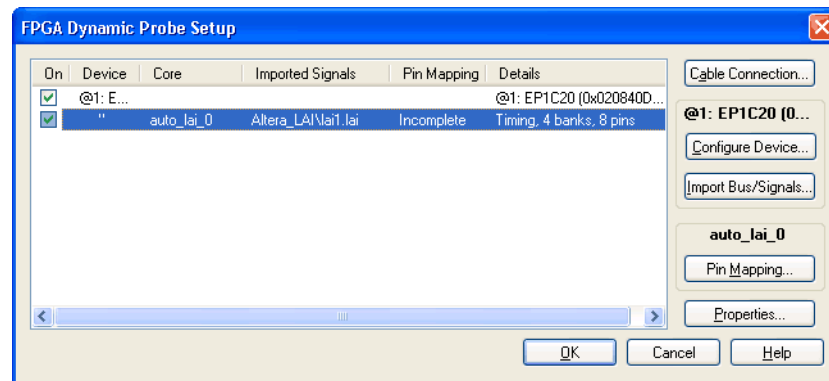
If you want to define buses/signals that apply to all banks, create them outside of the "FPGA Probe" folder. That way, the buses/signals are not associated with a bank.

Step 6. Map FPGA pins

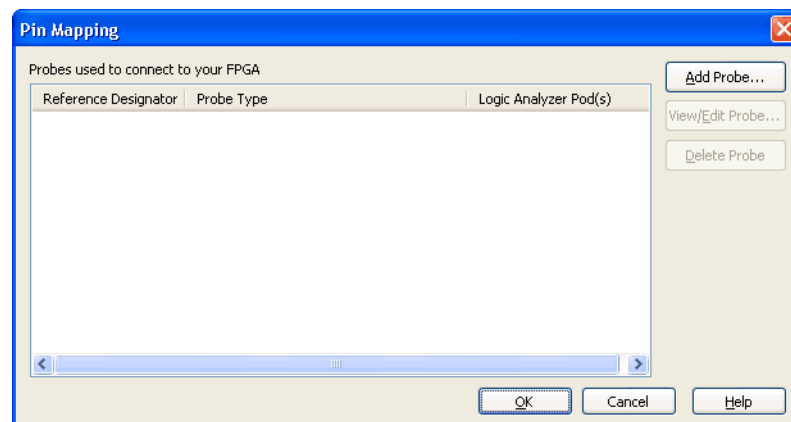
Quickly specify how the FPGA pins (the signal outputs of Altera LAI) are connected to your logic analyzer. Select your probe type and rapidly provide the information needed for the logic analyzer to automatically track names of signals routed through the Altera LAI core.

To map FPGA pins to logic analyzer probes:

- 1 In the FPGA Dynamic Probe Setup dialog (see [page 50](#)), select the Altera LAI core whose output pins you want to map; then, click **Pin Mapping...**

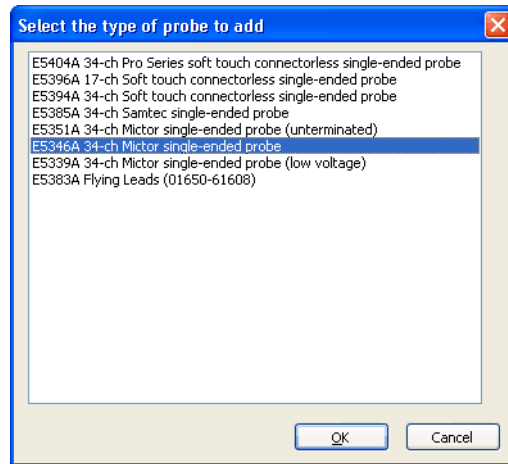


- 2 In the Pin Mapping dialog (see [page 51](#)), click **Add Probe...**



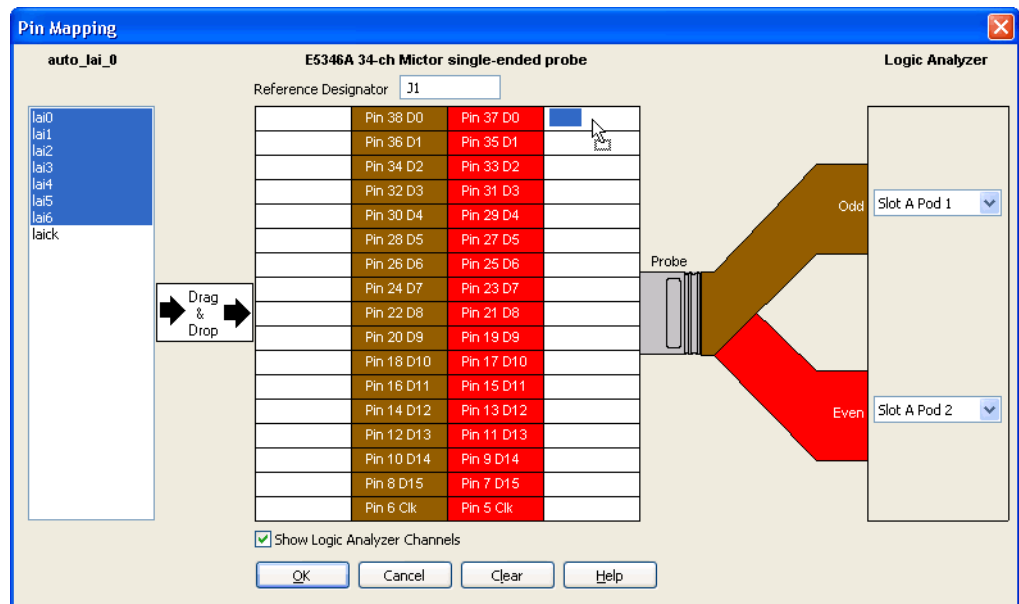
- 3 In the "Select the type of probe to add" dialog, select the type of probe that is used to connect to your FPGA; then, click **OK**.

6 Measurement Steps

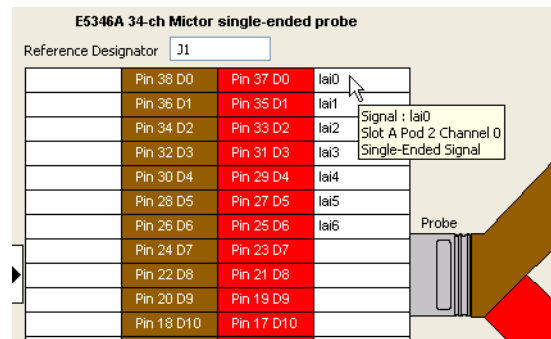


If your probe doesn't appear in the list, you can "download the latest probe definitions from the web" (in the online help).

- 4 In the Pin Mapping Edit dialog (see [page 52](#)), select the FPGA pins (you can select multiple pins using Shift-click or Ctrl-click) and drag them on to the pin/pad map.



After you've mapped FPGA pins to the probe, you can hover the mouse pointer over a pin description field to view a tool tip describing the FPGA debug pin name, the pod connection, the channel number, and the signal type (single-ended or differential).



You can clear all FPGA pins that have been mapped to pins/pads by clicking **Clear**. You can clear individual pin mappings by dragging a pin from the pin/pad diagram back to the FPGA Pins list.

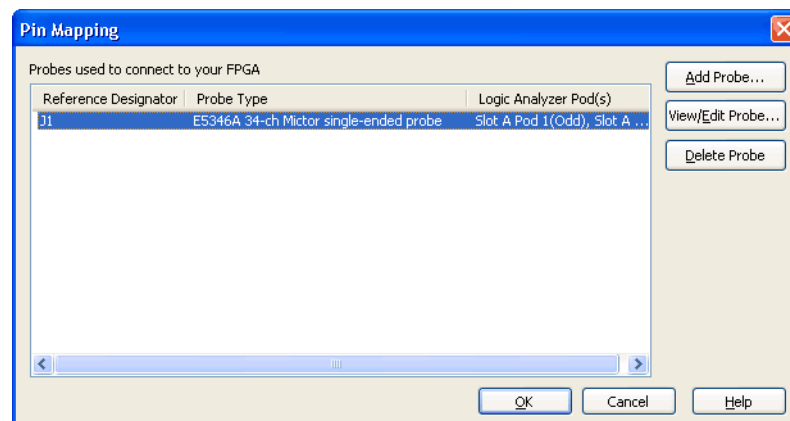
- 5 Select the logic analyzer pods that the probe is connected to.

When you wish to map multiple cores using different halves of the same probe, make sure you select **None** for the half that will be used by the other core.

NOTE

For state (synchronous) cores, you need to make sure that the ATCK pin maps to one of the "Clk" pin/pad locations (which identify clock signal inputs) and that the associated logic analyzer pod is valid for clock inputs. (In the *General State Mode*, the clock lines on the first 4 pods of a logic analyzer can be used as clock inputs; in the *Turbo State Mode*, the clock line on the first pod can be used as a clock input.)

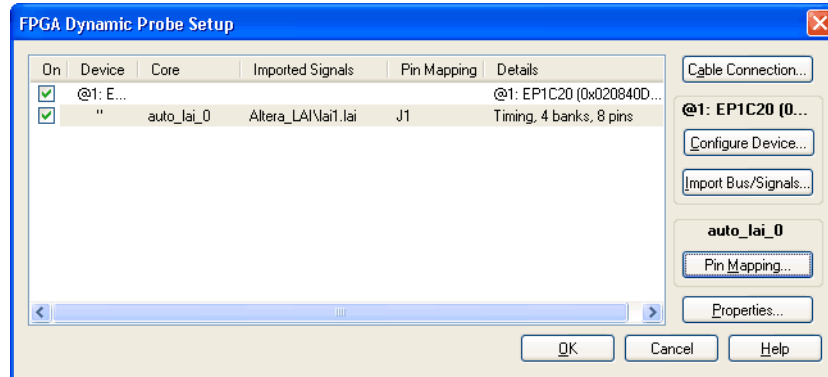
- 6 When you are done mapping FPGA pins, click **OK**. Note that your probe has been added to the list in the Pin Mapping dialog.



- 7 Click **OK** to close the Pin Mapping dialog.

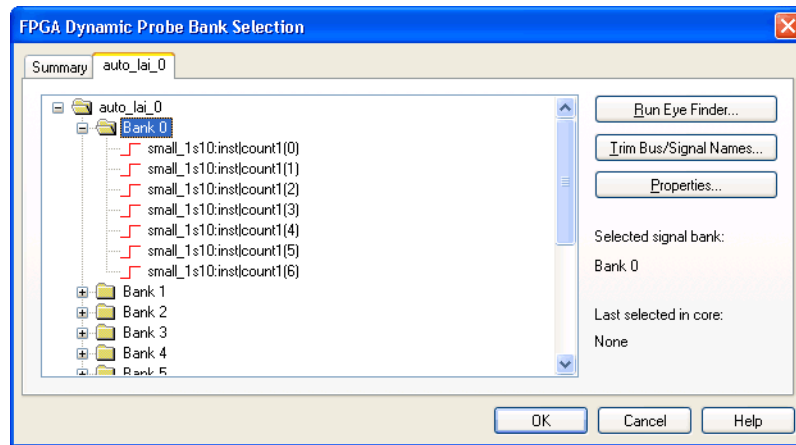
6 Measurement Steps

In the FPGA Dynamic Probe Setup dialog, notice pin mapping is no longer "Incomplete".



- 8 Click **OK** to close the FPGA Dynamic Probe Setup dialog.


The FPGA Dynamic Probe dialog opens automatically. If you expand a bank, you see the imported bus/signal names.

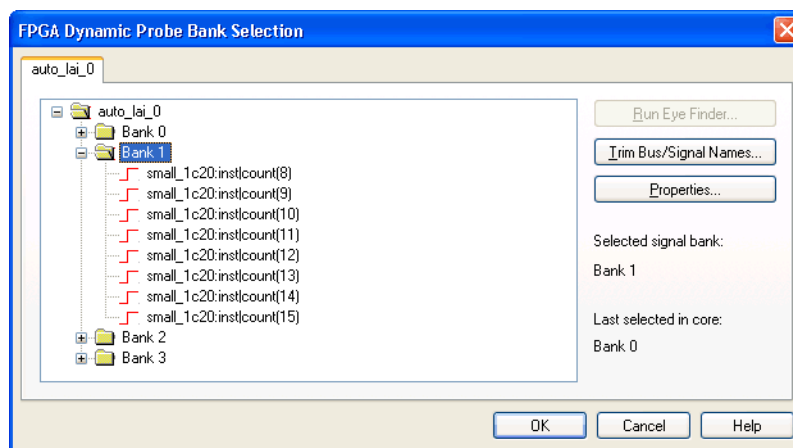


- Next** • Step 7. Make the measurement (see [page 39](#))

Step 7. Make the measurement

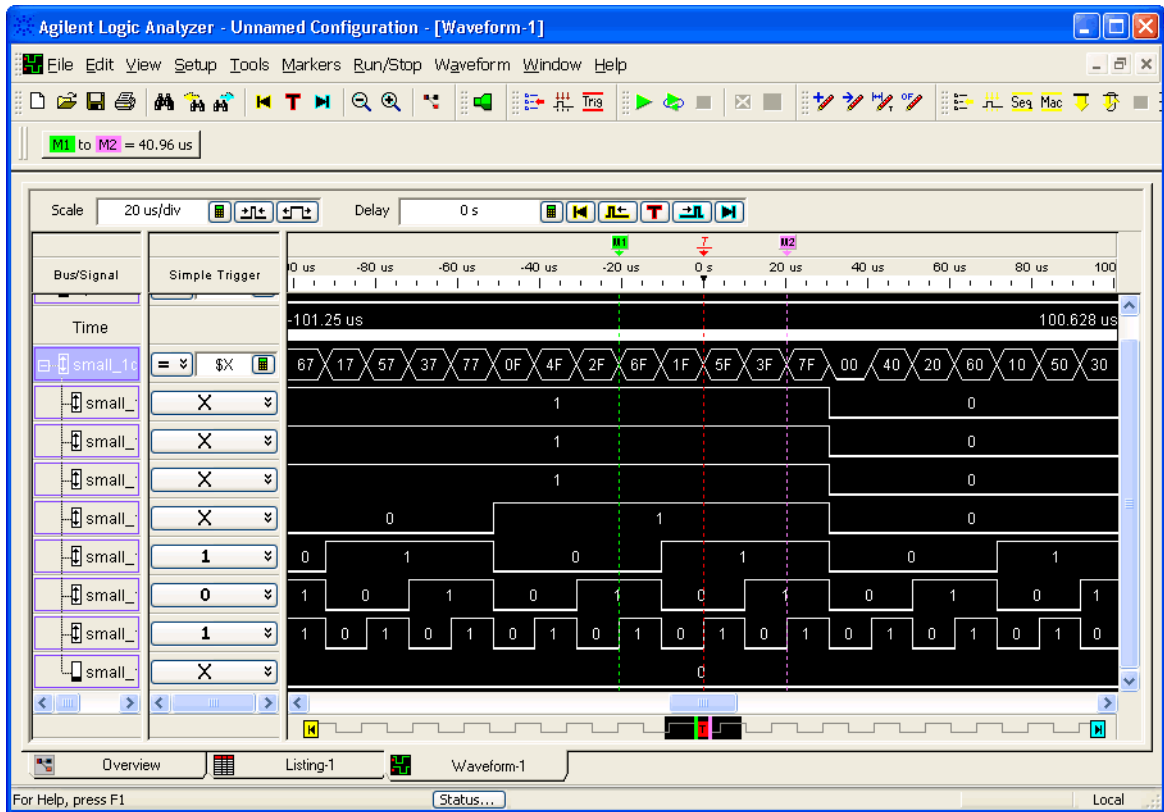
At this point, you are ready to use the logic analyzer (as you would normally) to capture activity on internal FPGA signals.

You can tell the Altera LAI core to switch signal banks without affecting the timing of your design. When viewing the Probes toolbar (**View>Toolbars>Probes**), click  to open the FPGA Dynamic Probe dialog. Then, select the signal bank to be routed to the logic analyzer and click **OK**. You can change signal banks as often as needed to make measurements throughout your FPGA.



You can correlate internal FPGA activity with external measurements. With each new selection of a signal bank, the application updates new signal names from your design to the logic analyzer. View internal FPGA activity and time correlate internal FPGA measurements with external events in the surrounding system.

6 Measurement Steps



NOTE

Timing zoom is automatically disabled when using the FPGA dynamic probe. You can re-enable timing zoom; however, because of the Altera LAI core, timing zoom does not provide an accurate representation of internal FPGA signals.

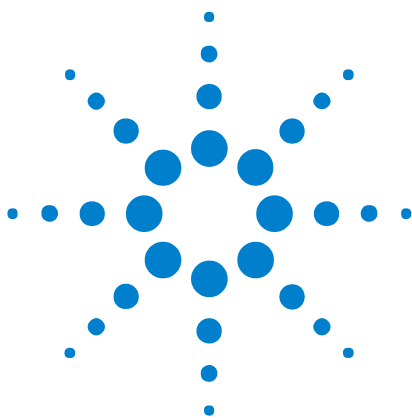
NOTE

Captured data is invalidated whenever you:

- Select a different bank.
- Select a different core.
- Download configuration bits into an FPGA.
- Reopen a cable connection.
- Imported signal names.
- Trim imported bus/signal names.
- Change the FPGA pin mapping.

See Also

- "Capturing Data from the Device Under Test" (in the online help)
- "Analyzing the Captured Data" (in the online help)

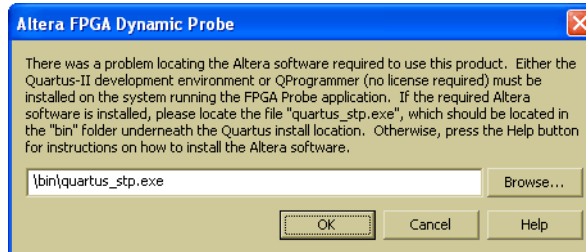


7 FPGA Dynamic Probe Troubleshooting

- When I click the 'Cable Connection' button I get 'problem locating Altera software' dialog (see [page 42](#))
- When I click the 'Cable Connection' button I get 'script error' dialog (see [page 43](#))
- If you don't see activity in the logic analyzer (see [page 44](#))
- If state mode measurements don't work (see [page 45](#))



When I click the 'Cable Connection' button I get 'problem locating Altera software' dialog



Possible cause: Default install path was changed during Quartus II installation. Actions:

- 1 Follow the instructions displayed on the dialog. If the file 'quartus_stp.exe' does not exist anywhere on the machine, continue with step 2.
- 2 Close the error and 'Cable Connection' dialogs.
- 3 Use Windows Add/Remove Programs to "Modify" the Quartus II installation, checking both the QProgrammer and SignalTap boxes before confirming. Reboot.

When I click the 'Cable Connection' button I get 'script error' dialog

NOTE

The blue light on the USB Blaster should blink when it is being identified.

Possible causes:

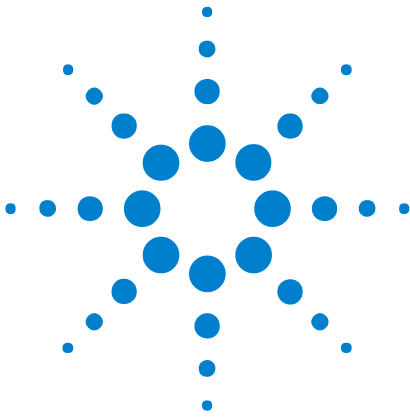
- There are no connected cables. Actions:
 - a** Close the error and 'Cable Connection' dialogs.
 - b** Re-seat the connection between the oscilloscope or PC and the Altera cable.
 - c** Retry the 'Cable Connection' button.
- Cable driver installation is incomplete. Actions:
 - a** Close the error and 'Cable Connection' dialogs.
 - b** Verify: Windows Device Manager should show a USB controller named "Altera USB-Blaster". If this controller has a red X, it is disabled. Right-click and select 'Enable'. If it has a yellow exclamation mark, then the Altera driver has not been fully installed. There is probably a New Hardware Found dialog hidden beneath the display. Complete the instructions on that dialog. See [To install the USB Blaster device driver \(see page 20\)](#)
 - c** Retry the 'Cable Connection' button.
- Selected cable not connected to DUT (device under test). Actions:
 - a** Close the error and 'Cable Connection' dialogs.
 - b** Re-seat connection between Altera cable and DUT (ensure plug on board is not reversed).
 - c** Retry the 'Cable Connection' button.
- DUT is not powered up. Actions:
 - a** Close the error dialog and 'Cable Connection' dialog.
 - b** Power up DUT.
 - c** Retry the 'Cable Connection' button.

If you don't see activity in the logic analyzer

If you get a dynamic status from the core that says everything is enabled and ready, but you see no activity on your logic analyzer, check your connections to and from your device under test to the logic analyzer pod cables.

If state mode measurements don't work

If you are unable to capture data in state mode, either look at the clock activity indicators and select the appropriate clock for state measurements, or make a timing measurement to determine which clock is the master clock.



8 FPGA Dynamic Probe Concepts

- Automated Logic Analyzer Set Up (see [page 48](#))

Automated Logic Analyzer Set Up

The FPGA dynamic probe automatically sets up the logic analyzer for the type of Altera LAI core it connects to.

For timing (asynchronous) cores, the FPGA dynamic probe automatically sets up:

- Timing mode.

For state (synchronous) cores, the FPGA dynamic probe automatically sets up:

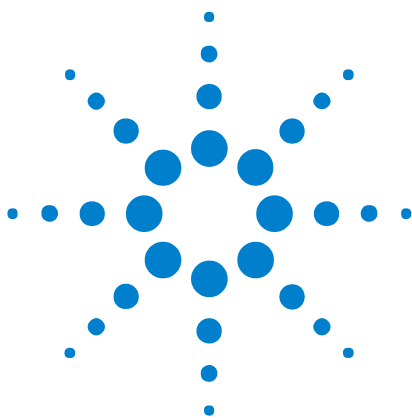
- State mode.
- Master clock mode.
- Clock signal and edge.

For all types of cores, the FPGA dynamic probe automatically sets up:

- Bus/signal names for the selected bank.

In the logic analyzer module's "Analyzer Setup dialog" (in the online help), you can rename buses/signals (see [page 32](#)) and define additional bus/signal names (see [page 33](#)), but changing any of the other settings made by the FPGA dynamic probe will interfere with its operation.

You are free to change settings that are untouched by the FPGA dynamic probe (like memory depth, trigger position, or sampling positions); they will not affect the FPGA dynamic probe.



9 FPGA Dynamic Probe Reference

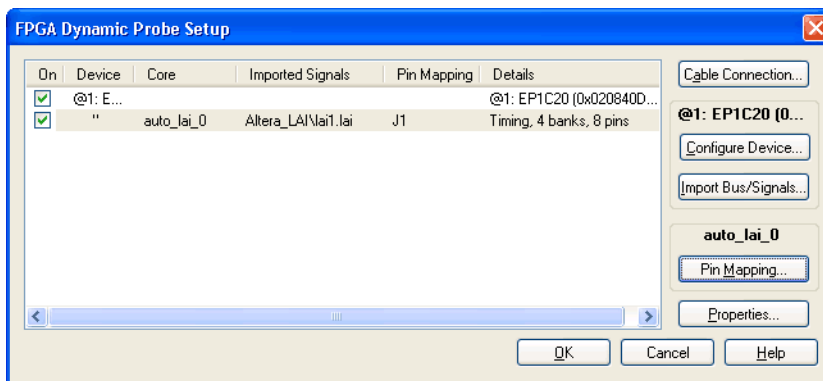
- FPGA Dynamic Probe Setup Dialog (see [page 50](#))
 - Cable Connection Dialog (see [page 51](#))
 - Pin Mapping Dialog (see [page 51](#))
 - Pin Mapping Edit Dialog (see [page 52](#))
 - Select FPGA Configuration File Dialog (see [page 54](#))
 - Select Signal Import File Dialog (see [page 54](#))
 - Properties Dialog (see [page 55](#))
 - Core Details Dialog (see [page 55](#))
- FPGA Dynamic Probe Bank Selection Dialog (see [page 57](#))
 - Trim Bus/Signal Names Dialog (see [page 57](#))
- Specifications and Characteristics (see [page 59](#))



FPGA Dynamic Probe Setup Dialog

The FPGA Dynamic Probe (see [page 9](#)) dialog lets you:

- Establish a connection between the logic analyzer and an FPGA with one or more Altera LAI cores.
- Configure the FPGA with a new design file.
- Map FPGA pins to probe pins/pads.
- Import signal names from the FPGA design tool.



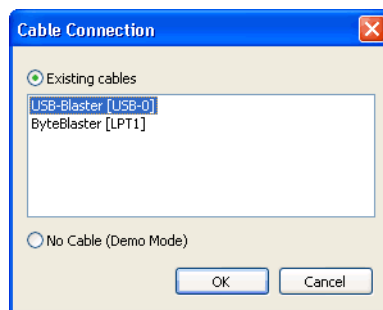
On (in FPGA device list)	The check boxes in this column let you enable or disable a core for use. If you do not want to use a particular core (typically in the multiple core case), you can uncheck its box, and the outputs of the core will be disabled. If a core's "always on" mode is enabled (see the core Details (see page 55) within its Properties dialog (see page 55)), the core is always enabled and can be probed at powerup (bank 0 will be the selected bank). In this case, the core cannot be disabled, and the check box cannot be unchecked.
Cable Connection...	Opens the Cable Connection dialog (see page 51) for establishing a connection between the logic analyzer and the Altera LAI core.
Configure Device...	Opens the Select FPGA Configuration File dialog (see page 54) for downloading a design into the selected FPGA device.
Import Bus/Signals...	Opens the Select Signal Import File dialog (see page 54) for importing internal FPGA bus/signal names.

Pin Mapping...	Opens the Pin Mapping dialog (see page 51) for defining the logic analyzer probes that are used to connect to the FPGA and setting up the pin mapping (see Step 6. Map FPGA pins (see page 35)).
Properties...	Opens the Properties dialog (see page 55) which lets you rename devices and cores as well as display information about the selected Altera LAI core.

See Also • [Measurement Steps](#) (see [page 27](#))

Cable Connection Dialog

The Cable Connection dialog lets you specify the the type of cable used to connect the logic analyzer to the device under test JTAG port.



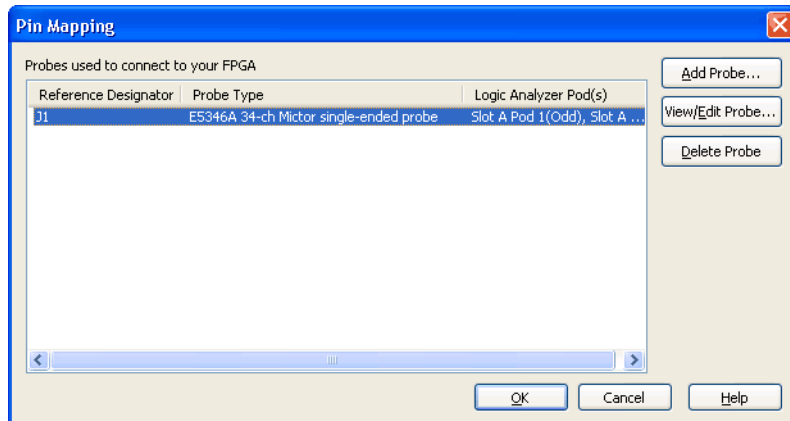
Existing cables	Lets you select a cable that has been set up using the Altera Quartus II Programmer (or design) software.
No Cable (Demo Mode)	Simulates a cable connection for demonstration purposes.

See Also • [Step 2. Set up the JTAG cable using the programmer software](#) (see [page 19](#))

- [Step 3. Establish connection between analyzer and JTAG cable](#) (see [page 28](#))

Pin Mapping Dialog

The Pin Mapping dialog lets you define the logic analyzer probes that are used to connect to the FPGA, and it lets you set up the FPGA pin to probe pin/pad mapping.

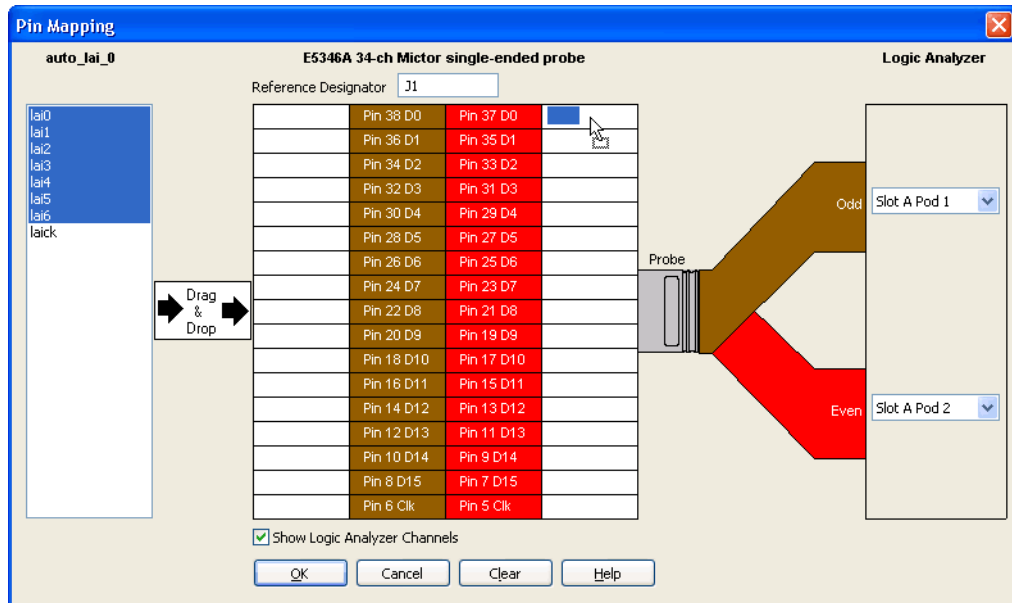


Add Probe...	Opens the "Select the type of probe to add" dialog; when you click OK , the Pin Mapping Edit dialog (see page 52) is opened for mapping the FPGA output pins to the probe pins/pads. If your probe doesn't appear in the list of probe types, you can "download the latest probe definitions from the web" (in the online help).
Edit Probe...	For the selected probe, opens the Pin Mapping Edit dialog (see page 52) for editing the FPGA output pins to probe pin/pad mapping.
Delete Probe	Deletes the selected probe.

See Also • Step 6. Map FPGA pins (see [page 35](#))

Pin Mapping Edit Dialog

The Pin Mapping Edit dialog lets you map the FPGA output pins to the logic analyzer probe pins/pads.

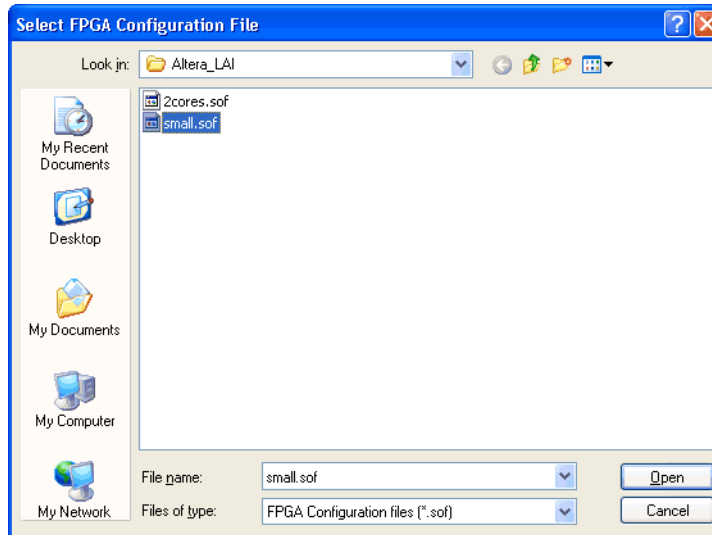


Reference Designator	Identifies the reference designator (in the device under test) of the probe connector, the connectorless probe retention module, or pins probed by flying leads.
FPGA Pins	Lists the FPGA pins used for the Altera LAI core outputs. When dragging these pins onto the pin/pad map, you can select multiple pins using Shift-click or Ctrl-click.
Probe Pin/Pad Diagram	Diagrams probe pins/pads, flying-lead channels, or termination adapter pins, and provides fields for dropping FPGA pin numbers.
Logic Analyzer Slot, Pod	Lets you select the logic analyzer module slots/pods to which the probe, flying leads, or termination adapter is connected.
Show Logic Analyzer Channels	When checked, the logic analyzer pod channel numbers are displayed in the probe pin/pad diagram next to the pin/pad numbers.
Clear	Clears all FPGA pins that have been mapped to pins/pads. You can clear individual pin mappings by dragging a pin from the pin/pad diagram back to the FPGA Pins list.

See Also • Step 7. Map FPGA pins (see [page 39](#))

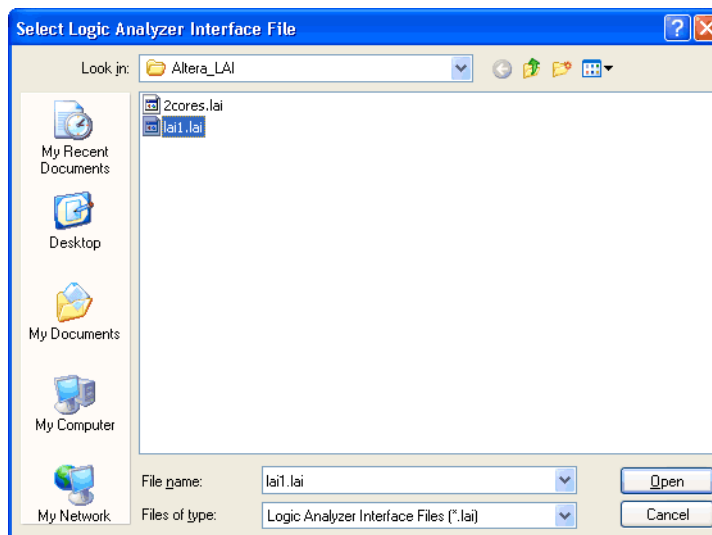
Select FPGA Configuration File Dialog

The Select FPGA Configuration File dialog lets you select a design file for downloading into an FPGA device on the JTAG chain.



Select Signal Import File Dialog

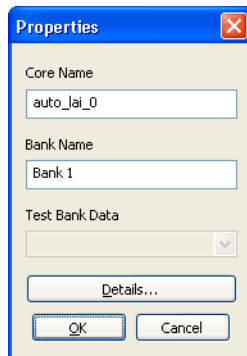
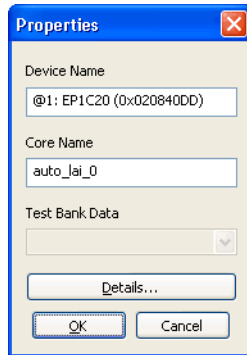
The Select Signal Import File dialog lets you select the file (from the FPGA design tool) that contains the names of the internal buses/signals that appear on Altera LAI core inputs.



See Also • Step 5. Import signal names (see [page 31](#))

Properties Dialog

The Properties dialog lets you change device, core, and bank names as well as view detailed information about the core.

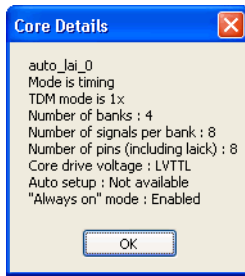


Device Name	Lets you rename the selected device.
Core Name	Lets you rename the selected core.
Bank Name	Lets you rename the selected bank.
Test Bank Data	Not available with Altera LAI cores.
Details...	Opens the Core Details dialog (see page 55) which displays information about the selected Altera LAI core.

Core Details Dialog

The Core Details dialog displays information about the selected Altera LAI core.

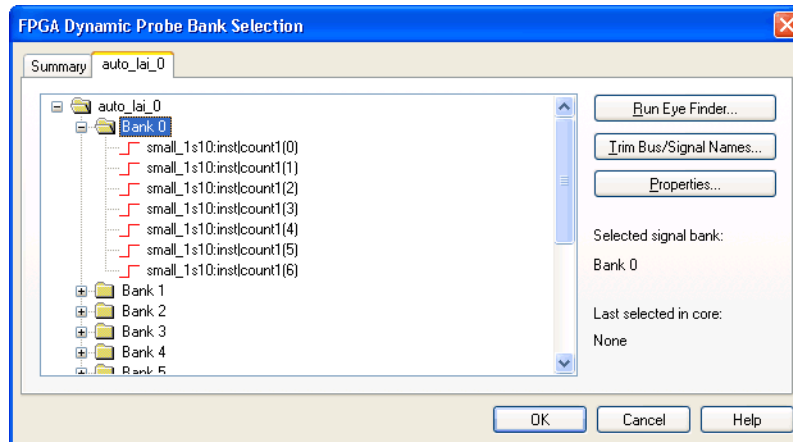
9 FPGA Dynamic Probe Reference



FPGA Dynamic Probe Bank Selection Dialog

The FPGA Dynamic Probe (see [page 9](#)) Bank Selection dialog lets you:

- Select a different bank of internal signals to probe.
- Rename individual signals (without having to do global trimming) by triple-clicking the signal name.

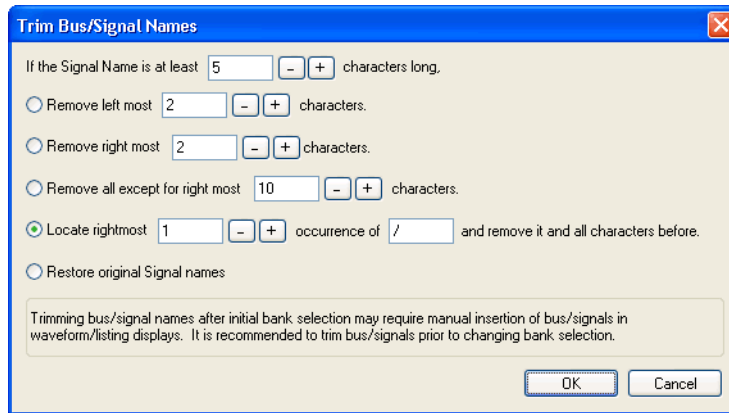


Run Eye Finder...	Opens the "Thresholds and Sample Positions dialog" (in the online help) for running <i>eye finder</i> to automatically adjust the state mode sampling positions. This button is available when probing only state (synchronous) cores. If there are any timing (asynchronous) cores, the logic analyzer is set up in timing mode, and <i>eye finder</i> is not available.
Trim Bus/Signal Names...	Opens the Trim Bus/Signal Names dialog (see page 57) for shortening imported FPGA internal bus/signal names.
Properties...	Opens the Properties dialog (see page 55) which lets you rename cores and banks as well as display information about the selected Altera LAI core.

See Also • Measurement Steps (see [page 27](#))

Trim Bus/Signal Names Dialog

The Trim Bus/Signal Names dialog lets you specify how imported bus/signal names should be shortened.



If the Signal Name is at least	Only bus/signal names longer than this value will be trimmed.
Remove left most	The number of characters to remove from the beginning of the names.
Remove right most	The number of characters to remove from the end of the names.
Remove all except right most	The number of characters to leave at the end of the names.
Locate right most Nth occurrence of the string	The string before which all characters from the names are stripped.
Restore original Signal names	Undoes the bus/signal name trimming.

See Also • Step 5. Import signal names (see [page 31](#))

Specifications and Characteristics

The FPGA dynamic probe for Altera FPGAs has these specifications and characteristics:

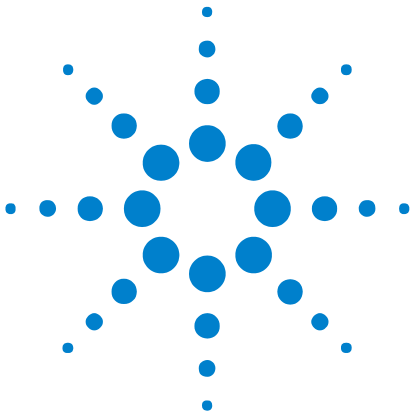
- Supported Logic Analyzers (see [page 59](#))
- FPGA Dynamic Probe Software Application (see [page 59](#))

Supported Logic Analyzers

Standalone logic analyzers:	1680 Series, 1690 Series, 16800 Series
Modular logic analysis systems:	16900A, 16901A, 16902A, 16902B, 16903A with one or more of the following cards: <ul style="list-style-type: none"> • 16740A, 16741A, 16742A. • 16750A, 16751A, 16752A, 16753A, 16754A, 16755A, 16756A. • 16760A. • 16910A, 16911A, 16950A, 16950B, 16951B. A single node-locked FPGA dynamic probe license will enable all modules within a 16900 Series system.
Triggering capabilities:	Determined by logic analyzer.
Supported probing mechanisms:	Soft touch (34-channel and 17-channel), Mictor, Samtec, Flying lead

FPGA Dynamic Probe Software Application

Maximum number of devices supported on a JTAG scan chain:	256
Maximum number of Altera LAI cores supported per FPGA device:	15



10 Probe Control, COM Automation

The *Agilent Logic Analyzer* application includes the COM Automation Server. This software lets you write programs that control the *Agilent Logic Analyzer* application from remote computers on the Local Area Network (LAN).

In a COM automation program, you can configure a probe by:

- Loading a configuration file (which configures the complete logic analyzer setup).
- Using the "Probe" (in the online help) object's "DoCommands" (in the online help) method with an XML-format string parameter (see Probe Setup, XML Format (see [page 63](#))).

You can get information about a probe's configuration using the Probe object's "QueryCommand" (in the online help) method. Queries supported by the FPGA dynamic probe are listed below.

For more information about logic analyzer COM automation and probe objects in general, see "COM Automation" (in the online help).

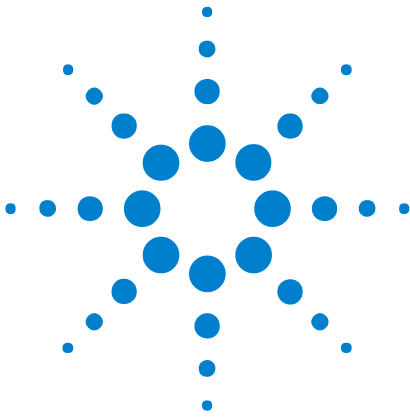
XML-Based Queries Supported

The FPGA dynamic probe supports the following XML-based queries (made with the "Probe" (in the online help) object's "QueryCommand" (in the online help) method).

Query	Description
GetAllSetup	Returns the current setup, using the full tag set, used for writing generic configuration files (see the XML format <Properties> element (see page 88)).
GetProperties	Returns the current setup, using the full tag set, equivalent to "GetAllSetup" (see the XML format <Properties> element (see page 88)).

- See Also**
- "COM Automation" (in the online help)
 - Probe Setup, XML Format (see [page 63](#))





11

Probe Setup, XML Format

When you save logic analyzer configurations to XML format files, setup information for the FPGA dynamic probe is included.

This XML format setup information is also used when writing COM automation programs to control the logic analyzer from a remote computer.

XML elements for the FPGA dynamic probe have the following hierarchy:

```
<Properties> (see page 88)
  <ATC_II> (see page 65)
  <JTAG_Chain> (see page 78)
  <Devices> (see page 77)
    <Device> (see page 75)
      <Cores> (see page 73)
        <Core> (see page 71)
          <Banks> (see page 70)
            <Bank> (see page 66)
              <Signals> (see page 92)
                <Signal> (see page 90)
                  <Labels> (see page 81)
                    <Label> (see page 79)
                  <NonATCLabels> (see page 82)
                    <Label> (see page 80)
                    <Assignment> (see page 64)
                <WindowInfo> (see page 97)
                <SymbolInfo> (see page 95)
                <TriggerInfo> (see page 96)
            <PinMapping> (see page 83)
          <DefinedProbes> (see page 74)
            <Probe> (see page 87)
              <Pods> (see page 86)
                <Pod> (see page 85)
              <Signals> (see page 94)
                <Signal> (see page 91)
```

- See Also**
- "XML Format" (in the online help)
 - Probe Control, COM Automation (see [page 61](#))



<Assignment> Element

The <Assignment> element describes the logic analyzer pod and channel assignments for a Label element (under NonATCLabels).

Attributes

Name	Description
Channel	'number'
Pod	'number'

Parents This element can have the following parents: <Label> (see [page 80](#)).

Example

```
<NonATCLabels>
  <Label Name='My Bus 2' Comment='' Handle='131'>
    <Assignment Pod='1' Channel='0' />
    <Assignment Pod='1' Channel='1' />
    <Assignment Pod='1' Channel='2' />
    <Assignment Pod='1' Channel='3' />
    <Assignment Pod='1' Channel='4' />
    <Assignment Pod='1' Channel='5' />
    <Assignment Pod='1' Channel='6' />
    <Assignment Pod='1' Channel='7' />
  </Label>
</NonATCLabels>
```


<ATC_II> Element

The <ATC_II> element describes the selected device, the selected core, and the cable type.

Attributes

Name	Description
CableType	'number'
ParallelCablePort	'number'
ParallelCableSpeed	'number'
ParallelCableType	'number'
SelectedCore	'number'
SelectedDevice	'number'
USBCableSpeed	'number'

Parents This element can have the following parents: <Properties> (see [page 88](#)).

Example

```
<ATC_II SelectedDevice='1' SelectedCore='0' CableType='0'
  ParallelCableType='0' ParallelCableSpeed='2' ParallelCablePort='0'
  USBCableSpeed='0' />
```

<Bank> Element

The <Bank> element describes a bank within an Altera LAI core.

Attributes

Name	Description
CalibrationBank	'F' (false) or 'T' (true)
Name	'string'
NumDataPins	'number'
State2X	'F' (false) or 'T' (true)

Children This element can have the following children: <Signals> (see [page 92](#)), <NonATCLabels> (see [page 82](#)), <WindowInfo> (see [page 97](#)), <SymbolInfo> (see [page 95](#)), <TriggerInfo> (see [page 96](#)).

Parents This element can have the following parents: <Banks> (see [page 70](#)).

Example

```
<Bank Name='Bank-0' CalibrationBank='F' NumDataPins='16' State2X='F'>
  <Signals>
    <Signal>
      <Labels>
        <Label Name='/s2mon/tid' Bit='0' />
      </Labels>
    </Signal>
    <Signal>
      <Labels>
        <Label Name='/s2mon/tid' Bit='1' />
      </Labels>
    </Signal>
    <Signal>
      <Labels>
        <Label Name='/s2mon/tid' Bit='2' />
      </Labels>
    </Signal>
    <Signal>
      <Labels>
        <Label Name='/s2mon/tid' Bit='3' />
      </Labels>
    </Signal>
    <Signal>
      <Labels>
        <Label Name='/s2mon/tid' Bit='4' />
      </Labels>
    </Signal>
    <Signal>
      <Labels>
        <Label Name='/s2mon/tid' Bit='5' />
      </Labels>
    </Signal>
  </Signals>
</Bank>
```

```

    <Labels>
      <Label Name='/s2mon/tid' Bit='6' />
    </Labels>
  </Signal>
<Signal>
  <Labels>
    <Label Name='/s2mon/tid' Bit='7' />
  </Labels>
</Signal>
<Signal>
  <Labels>
    <Label Name='/s2mon/lastackid' Bit='0' />
  </Labels>
</Signal>
<Signal>
  <Labels>
    <Label Name='/s2mon/lastackid' Bit='1' />
  </Labels>
</Signal>
<Signal>
  <Labels>
    <Label Name='/s2mon/lastackid' Bit='2' />
  </Labels>
</Signal>
<Signal>
  <Labels>
    <Label Name='/s2mon/lastackid' Bit='3' />
  </Labels>
</Signal>
<Signal>
  <Labels>
    <Label Name='/s2mon/lastackid' Bit='4' />
  </Labels>
</Signal>
<Signal>
  <Labels>
    <Label Name='/s2mon/lastackid' Bit='5' />
  </Labels>
</Signal>
<Signal>
  <Labels>
    <Label Name='/s2mon/lastackid' Bit='6' />
  </Labels>
</Signal>
<Signal>
  <Labels />
</Signal>
</Signals>
<NonATCLabels />
<WindowInfo WindowHandle='1' WindowSettings='
&lt;Setup&gt;
  &lt;Sampling PerDivision=&apos;5 ns&apos;
    Delay=&apos;0 s&apos;/&gt;
&lt;BusSignals&gt;
  &lt;Clear/&gt;
  &lt;BusSignal Module=&apos;My 1682D-1&apos;
    Name=&apos;My Bus 1&apos; DefaultBase=&apos;Hex&apos;

```

```

        Color=&apos;hFFFFFF&apos; Height=&apos;30&apos;/&gt;
    &lt;BusSignal Module=&apos;My 1682D-1&apos;
        Name=&apos;/s2mon/tid&apos; DefaultBase=&apos;Hex&apos;
        Color=&apos;hFFFFFF&apos; Height=&apos;30&apos;/&gt;
    &lt;BusSignal Module=&apos;My 1682D-1&apos;
        Name=&apos;/s2mon/s2mstate&apos;
        DefaultBase=&apos;Hex&apos; Color=&apos;hFFFFFF&apos;
        Height=&apos;30&apos;/&gt;
    &lt;BusSignal Name=&apos;Time&apos; Color=&apos;hFFFFFF&apos;
        Height=&apos;30&apos;/&gt;
    &lt;/BusSignals&gt;
&lt;/Setup&gt;
' />
<WindowInfo WindowHandle='2' WindowSettings='
&lt;BusSignals&gt;
    &lt;Clear&gt;
    &lt;BusSignal Module=&apos;My 1682D-1&apos;
        Name=&apos;Sample Number&apos; Color=&apos;hFFFFFF&apos;
        Alignment=&apos;Right&apos; Width=&apos;112&apos;/&gt;
    &lt;BusSignal Module=&apos;My 1682D-1&apos;
        Name=&apos;My Bus 1&apos; DefaultBase=&apos;Hex&apos;
        Color=&apos;hFFFFFF&apos; Alignment=&apos;Right&apos;
        Width=&apos;113&apos;/&gt;
    &lt;BusSignal Name=&apos;Time&apos;
        DefaultBase=&apos;Absolute&apos; Color=&apos;hFFFFFF&apos;
        Alignment=&apos;Right&apos; Width=&apos;152&apos;/&gt;
    &lt;BusSignal Module=&apos;My 1682D-1&apos;
        Name=&apos;/s2mon/tid&apos; DefaultBase=&apos;Hex&apos;
        Color=&apos;hFFFFFF&apos; Alignment=&apos;Right&apos;
        Width=&apos;113&apos;/&gt;
    &lt;BusSignal Module=&apos;My 1682D-1&apos;
        Name=&apos;/s2mon/s2mstate&apos;
        DefaultBase=&apos;Hex&apos; Color=&apos;hFFFFFF&apos;
        Alignment=&apos;Right&apos; Width=&apos;120&apos;/&gt;
&lt;/BusSignals&gt;
' />
<SymbolInfo ModuleHandle='1' SymbolSettings='
&lt;Module&gt;
    &lt;BusSignalSetup&gt;
        &lt;BusSignals&gt;
            &lt;BusSignal Name=&apos;My Bus 1&apos;/&gt;
            &lt;Folder Name=&apos;Core 0 FPGA Probe&apos;
                Comment=&apos;Created by FPGA Dynamic Probe-1&apos;&gt;
            &lt;BusSignal Name=&apos;/s2mon/tid&apos;/&gt;
            &lt;BusSignal Name=&apos;/s2mon/s2mstate&apos;/&gt;
        &lt;/Folder&gt;
    &lt;/BusSignals&gt;
    &lt;NetlistImport&/&gt;
&lt;/BusSignalSetup&gt;
    &lt;Config TimeOfTrigger=&apos;1.110240661 Gs&apos;
        CorrelatedTriggerTime=&apos;0 s&apos;
        UserSkewTime=&apos;0 s&apos;
        SystemTrigger=&apos;T&apos;/&gt;
&lt;/Module&gt;
' />
<TriggerInfo ModuleHandle='1' TriggerSettings='
&lt;Module&gt;

```

```

<lt;Trigger Mode=&apos;State&apos; Type=&apos;Normal&apos;&gt;
  <lt;StoreQual Mode=&apos;Custom&apos;&gt;
    <lt;Event ParensNeeded=&apos;F&apos;&gt;
      <lt;Anything/&gt;
    <lt;/Event&gt;
  <lt;/StoreQual&gt;
  <lt;Step Number=&apos;1&apos;&gt;
    <lt;If&gt;
      <lt;Event ParensNeeded=&apos;F&apos;&gt;
        <lt;BusSignal Name=&apos;/s2mon/tid&apos;
          Bit=&apos;All&apos; Operator=&apos;Equals&apos;
          Value=&apos;h3F&apos;/&gt;
        <lt;/Event&gt;
        <lt;Occurrence Value=&apos;1&apos;
          Mode=&apos;Eventual&apos;/&gt;
        <lt;Action&gt;
          <lt;TriggerAction Operator=&apos;Fill Memory&apos;&gt;
            <lt;StoreQual Mode=&apos;Custom&apos;&gt;
              <lt;Event ParensNeeded=&apos;F&apos;&gt;
                <lt;DefaultStore/&gt;
              <lt;/Event&gt;
            <lt;/StoreQual&gt;
          <lt;/TriggerAction&gt;
        <lt;/Action&gt;
      <lt;/If&gt;
    <lt;/Step&gt;
  <lt;/Trigger&gt;
  <lt;Config TimeOfTrigger=&apos;1.110240661 Gs&apos;
    CorrelatedTriggerTime=&apos;0 s&apos;
    UserSkewTime=&apos;0 s&apos;
    SystemTrigger=&apos;T&apos;/&gt;
<lt;/Module&gt;
' />
</Bank>

```

<Banks> Element

The <Banks> element contains descriptions of banks within an Altera LAI core.

Children This element can have the following children: <Bank> (see [page 66](#)).

Parents This element can have the following parents: <Core> (see [page 71](#)).

Example

```
<Banks>
  <Bank Name='Bank 0' CalibrationBank='F' NumDataPins='16' State2X='F'>
    ...
  </Bank>
  <Bank Name='Bank 1' CalibrationBank='F' NumDataPins='16' State2X='F'>
    ...
  </Bank>
  <Bank Name='Bank 2' CalibrationBank='F' NumDataPins='16' State2X='F'>
    ...
  </Bank>
  <Bank Name='Bank 3' CalibrationBank='F' NumDataPins='16' State2X='F'>
    ...
  </Bank>
  <Bank Name='Test Bank' CalibrationBank='T' NumDataPins='16'
    State2X='F'>
    ...
  </Bank>
</Banks>
```

<Core> Element

The <Core> element describes a core within a device on the JTAG chain.

Attributes

Name	Description
ClockPodIndex	'number'
CoreCannotBeMaster	'F' (false) or 'T' (true)
CoreIsMaster	'F' (false) or 'T' (true)
Latency	'number'
MinimumPeriod	'number'
Name	'string'
NumBanks	'number'
NumPins	'number'
NumSignals	'number'
SelectedBank	'number'
SelectedForUse	'F' (false) or 'T' (true)
SelectedSignal	'number'
StateMode	'F' (false) or 'T' (true)
TDM_1X	'F' (false) or 'T' (true)
TestBankAvailable	'F' (false) or 'T' (true)
TestBankMode	'number'
Type	'number'
ThresholdCode	'number'

Children This element can have the following children: <Banks> (see [page 70](#)), <PinMapping> (see [page 83](#)).

Parents This element can have the following parents: <Cores> (see [page 73](#)).

Example

```
<Core Name='Core-1' Type='0' SelectedBank='0' SelectedSignal='-1'
  NumBanks='5' NumSignals='16' NumPins='17' StateMode='T' TDM_1X='T'
  ThresholdCode='92' TestBankAvailable='T' ClockPodIndex='0'
  SelectedForUse='T' CoreIsMaster='T' CoreCannotBeMaster='F'
  MinimumPeriod='-1' TestBankMode='2' Latency='4'>
  <Banks>
    <Bank Name='Bank 0' CalibrationBank='F' NumDataPins='16'
      State2X='F'>
      ...
    </Bank>
    <Bank Name='Bank 1' CalibrationBank='F' NumDataPins='16'
```

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```
        State2X='F'>
    ...
</Bank>
<Bank Name='Bank 2' CalibrationBank='F' NumDataPins='16'
    State2X='F'>
    ...
</Bank>
<Bank Name='Bank 3' CalibrationBank='F' NumDataPins='16'
    State2X='F'>
    ...
</Bank>
<Bank Name='Test Bank' CalibrationBank='T' NumDataPins='16'
    State2X='F'>
    ...
</Bank>
</Banks>
<PinMapping Attached='T' ModuleHandle='1'>
    <DefinedProbes>
        <Probe Name='J1' Type='E5346A 34-ch Mictor single-ended probe'>
            <Pods>
                <Pod Index='0' />
                <Pod Index='1' />
            </Pods>
            <Signals>
                ...
            </Signals>
        </Probe>
    </DefinedProbes>
</PinMapping>
</Core>
```


<Cores> Element

The <Cores> element contains descriptions of cores within a device on the JTAG chain.

Children This element can have the following children: <Core> (see [page 71](#)).

Parents This element can have the following parents: <Device> (see [page 75](#)).

Example

```
<Cores>
  <Core Name='Core 0' Type='0' SelectedBank='0' SelectedSignal='-1'
    NumBanks='5' NumSignals='16' NumPins='9' StateMode='T'
    TDM_1X='F' ThresholdCode='92' TestBankAvailable='T'
    ClockPodIndex='0' SelectedForUse='T' CoreIsMaster='F'
    CoreCannotBeMaster='F' MinimumPeriod='-1' TestBankMode='2'
    Latency='4'>
    <Banks>
      ...
    </Banks>
    <PinMapping Attached='T' ModuleHandle='1'>
      ...
    </PinMapping>
  </Core>
  <Core Name='Core 1' Type='0' SelectedBank='0' SelectedSignal='-1'
    NumBanks='2' NumSignals='9' NumPins='9' StateMode='F'
    TDM_1X='T' ThresholdCode='92' TestBankAvailable='F'
    ClockPodIndex='2' SelectedForUse='T' CoreIsMaster='T'
    CoreCannotBeMaster='F' MinimumPeriod='-1' TestBankMode='0'>
    <Banks>
      ...
    </Banks>
    <PinMapping Attached='T' ModuleHandle='1'>
      ...
    </PinMapping>
  </Core>
</Cores>
```

<DefinedProbes> Element

The <DefinedProbes> element contains defined probes.

Children This element can have the following children: <Probe> (see [page 87](#)).

Parents This element can have the following parents: <PinMapping> (see [page 83](#)).

Example

```
<DefinedProbes>
  <Probe Name='J1' Type='E5346A 34-ch Mictor single-ended probe'>
    <Pods>
      <Pod Index='0' />
      <Pod Index='1' />
    </Pods>
    <Signals>
      <Signal Name='ATD0' Pin='38' PinMapIndex='0'
        ClockChannel='F' />
      <Signal Name='ATD1' Pin='36' PinMapIndex='1'
        ClockChannel='F' />
      <Signal Name='ATD2' Pin='34' PinMapIndex='2'
        ClockChannel='F' />
      <Signal Name='ATD3' Pin='32' PinMapIndex='3'
        ClockChannel='F' />
      <Signal Name='ATD4' Pin='30' PinMapIndex='4'
        ClockChannel='F' />
      <Signal Name='ATD5' Pin='28' PinMapIndex='5'
        ClockChannel='F' />
      <Signal Name='ATD6' Pin='26' PinMapIndex='6'
        ClockChannel='F' />
      <Signal Name='ATD7' Pin='24' PinMapIndex='7'
        ClockChannel='F' />
      <Signal Name='ATD8' Pin='22' PinMapIndex='8'
        ClockChannel='F' />
      <Signal Name='ATD9' Pin='20' PinMapIndex='9'
        ClockChannel='F' />
      <Signal Name='ATD10' Pin='18' PinMapIndex='10'
        ClockChannel='F' />
      <Signal Name='ATD11' Pin='16' PinMapIndex='11'
        ClockChannel='F' />
      <Signal Name='ATD12' Pin='14' PinMapIndex='12'
        ClockChannel='F' />
      <Signal Name='ATD13' Pin='12' PinMapIndex='13'
        ClockChannel='F' />
      <Signal Name='ATD14' Pin='10' PinMapIndex='14'
        ClockChannel='F' />
      <Signal Name='ATCK' Pin='6' PinMapIndex='16'
        ClockChannel='T' />
    </Signals>
  </Probe>
</DefinedProbes>
```

<Device> Element

The <Device> element describes a device on the JTAG chain.

Attributes

Name	Description
CDCFilename	'string'
Configurable	'F' (false) or 'T' (true)
FPGAFilename	'string'
IRLength	'number'
Name	'string'
NumCores	'number'
SelectedForUse	'F' (false) or 'T' (true)
Type	'number'
UserRegNum	'number'

Children This element can have the following children: <Cores> (see [page 73](#)).

Parents This element can have the following parents: <Devices> (see [page 77](#)).

Example

```
<Device Name='Device 1' Type='0' NumCores='2' UserRegNum='1'
  Configurable='T' IRLength='6' CDCFilename='C:\Documents and
  Settings\user\My Documents\Agilent Technologies\Logic
  Analyzer\Config Files\demo\Altera_demo_V8.cdc'
  FPGAFilename='C:\Documents and Settings\user\My Documents\Agilent
  Technologies\Logic Analyzer\Config Files\demo\Altera_demo_V8.bit'
  SelectedForUse='F'>
  <Cores>
    <Core Name='Core 0' Type='0' SelectedBank='0' SelectedSignal='-1'
      NumBanks='5' NumSignals='16' NumPins='9' StateMode='T'
      TDM_1X='F' ThresholdCode='92' TestBankAvailable='T'
      ClockPodIndex='0' SelectedForUse='T' CoreIsMaster='F'
      CoreCannotBeMaster='F' MinimumPeriod='-1' TestBankMode='2'
      Latency='4'>
      <Banks>
        ...
      </Banks>
      <PinMapping Attached='T' ModuleHandle='1'>
        ...
      </PinMapping>
    </Core>
    <Core Name='Core 1' Type='0' SelectedBank='0' SelectedSignal='-1'
      NumBanks='2' NumSignals='9' NumPins='9' StateMode='F'
      TDM_1X='T' ThresholdCode='92' TestBankAvailable='F'
      ClockPodIndex='2' SelectedForUse='T' CoreIsMaster='T'
      CoreCannotBeMaster='F' MinimumPeriod='-1' TestBankMode='0'>
      <Banks>
        ...
      </Banks>
    </Core>
  </Cores>
</Device>
```

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```
    </Banks>
    <PinMapping Attached='T' ModuleHandle='1'>
      ...
    </PinMapping>
  </Core>
</Cores>
</Device>
```

<Devices> Element

The <Devices> element contains descriptions of the devices on the JTAG chain.

Children This element can have the following children: <Device> (see [page 75](#)).

Parents This element can have the following parents: <Properties> (see [page 88](#)).

Example

```
<Devices>
  <Device Name='Device 0' Type='0' NumCores='0' UserRegNum='0'
    Configurable='F' IRLength='8' CDCFilename='' FPGAFilename=''
    SelectedForUse='F'>
    <Cores/>
  </Device>
  <Device Name='Device 1' Type='0' NumCores='2' UserRegNum='1'
    Configurable='T' IRLength='6' CDCFilename='C:\Documents and
    Settings\user\My Documents\Agilent Technologies\Logic
    Analyzer\Config Files\demo\Altera_demo_V8.cdc'
    FPGAFilename='C:\Documents and Settings\user\My
    Documents\Agilent Technologies\Logic Analyzer\Config
    Files\demo\Altera_demo_V8.bit' SelectedForUse='F'>
    <Cores>
      <Core Name='Core 0' Type='0' SelectedBank='0'
        SelectedSignal='-1' NumBanks='5' NumSignals='16'
        NumPins='9' StateMode='T' TDM_1X='F' ThresholdCode='92'
        TestBankAvailable='T' ClockPodIndex='0'
        SelectedForUse='T' CoreIsMaster='F'
        CoreCannotBeMaster='F' MinimumPeriod='-1'
        TestBankMode='2' Latency='4'>
        <Banks>
          ...
        </Banks>
        <PinMapping Attached='T' ModuleHandle='1'>
          ...
        </PinMapping>
      </Core>
      <Core Name='Core 1' Type='0' SelectedBank='0'
        SelectedSignal='-1' NumBanks='2' NumSignals='9'
        NumPins='9' StateMode='F' TDM_1X='T' ThresholdCode='92'
        TestBankAvailable='F' ClockPodIndex='2'
        SelectedForUse='T' CoreIsMaster='T'
        CoreCannotBeMaster='F' MinimumPeriod='-1'
        TestBankMode='0'>
        <Banks>
          ...
        </Banks>
        <PinMapping Attached='T' ModuleHandle='1'>
          ...
        </PinMapping>
      </Core>
    </Cores>
  </Device>
</Devices>
```

<JTAG_Chain> Element

The <JTAG_Chain> element describes the number of devices and the number of Altera LAI cores on the JTAG chain.

Attributes

Name	Description
NumATC_II	'number'
NumDevices	'number'

Parents This element can have the following parents: <Properties> (see [page 88](#)).

Example `<JTAG_Chain NumDevices='3' NumATC_II='2' />`

<Label> Element

The <Label> element describes a label within a signal.

Attributes

Name	Description
Bit	'number'
Name	'string'

Parents This element can have the following parents: <Labels> (see [page 81](#)).

Example <Label Name='/s2mon/tid' Bit='0' />

<Label> Element (under NonATCLabels)

The <Label> element describes a bus/signal name within the NonATCLabels element.

Attributes

Name	Description
Comment	'string'
Handle	'number'
Name	'string'

Children This element can have the following children: <Assignment> (see [page 64](#)).

Parents This element can have the following parents: <NonATCLabels> (see [page 82](#)).

Example

```
<NonATCLabels>
  <Label Name='My Bus 2' Comment='' Handle='131'>
    <Assignment Pod='1' Channel='0' />
    <Assignment Pod='1' Channel='1' />
    <Assignment Pod='1' Channel='2' />
    <Assignment Pod='1' Channel='3' />
    <Assignment Pod='1' Channel='4' />
    <Assignment Pod='1' Channel='5' />
    <Assignment Pod='1' Channel='6' />
    <Assignment Pod='1' Channel='7' />
  </Label>
</NonATCLabels>
```


<Labels> Element

The <Labels> element contains descriptions of labels within a signal.

Children This element can have the following children: <Label> (see [page 79](#)).

Parents This element can have the following parents: <Signal> (see [page 90](#)).

Example

```
<Labels>
  <Label Name='/s2mon/tid' Bit='0' />
</Labels>
```

<NonATCLabels> Element

The <NonATCLabels> element contains a bank's bus/signal names that were not imported from a .cdc file or were renamed (for example, the Calibration Bus or any other renamed or additionally defined bus/signal names).

Children This element can have the following children: <Label> (see [page 80](#)).

Parents This element can have the following parents: <Bank> (see [page 66](#)).

Example

```
<NonATCLabels>
  <Label Name='My Bus 2' Comment='' Handle='131'>
    <Assignment Pod='1' Channel='0' />
    <Assignment Pod='1' Channel='1' />
    <Assignment Pod='1' Channel='2' />
    <Assignment Pod='1' Channel='3' />
    <Assignment Pod='1' Channel='4' />
    <Assignment Pod='1' Channel='5' />
    <Assignment Pod='1' Channel='6' />
    <Assignment Pod='1' Channel='7' />
  </Label>
</NonATCLabels>
```

<PinMapping> Element

The <PinMapping> element contains descriptions of pin mapping within an Altera LAI core.

Attributes

Name	Description
Attached	'F' (false) or 'T' (true)
ModuleHandle	'number'

Children This element can have the following children: <DefinedProbes> (see [page 74](#)).

Parents This element can have the following parents: <Core> (see [page 71](#)).

Example

```
<PinMapping Attached='T' ModuleHandle='1'>
  <DefinedProbes>
    <Probe Name='J1' Type='E5346A 34-ch Mictor single-ended probe'>
      <Pods>
        <Pod Index='0' />
        <Pod Index='1' />
      </Pods>
      <Signals>
        <Signal Name='ATD0' Pin='38' PinMapIndex='0'
          ClockChannel='F' />
        <Signal Name='ATD1' Pin='36' PinMapIndex='1'
          ClockChannel='F' />
        <Signal Name='ATD2' Pin='34' PinMapIndex='2'
          ClockChannel='F' />
        <Signal Name='ATD3' Pin='32' PinMapIndex='3'
          ClockChannel='F' />
        <Signal Name='ATD4' Pin='30' PinMapIndex='4'
          ClockChannel='F' />
        <Signal Name='ATD5' Pin='28' PinMapIndex='5'
          ClockChannel='F' />
        <Signal Name='ATD6' Pin='26' PinMapIndex='6'
          ClockChannel='F' />
        <Signal Name='ATD7' Pin='24' PinMapIndex='7'
          ClockChannel='F' />
        <Signal Name='ATD8' Pin='22' PinMapIndex='8'
          ClockChannel='F' />
        <Signal Name='ATD9' Pin='20' PinMapIndex='9'
          ClockChannel='F' />
        <Signal Name='ATD10' Pin='18' PinMapIndex='10'
          ClockChannel='F' />
        <Signal Name='ATD11' Pin='16' PinMapIndex='11'
          ClockChannel='F' />
        <Signal Name='ATD12' Pin='14' PinMapIndex='12'
          ClockChannel='F' />
        <Signal Name='ATD13' Pin='12' PinMapIndex='13'
          ClockChannel='F' />
        <Signal Name='ATD14' Pin='10' PinMapIndex='14'
```

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```
        ClockChannel='F' />
    <Signal Name='ATCK' Pin='6' PinMapIndex='16'
        ClockChannel='T' />
    </Signals>
</Probe>
</DefinedProbes>
</PinMapping>
```

<Pod> Element

The <Pod> element describes the pod index used within a defined probe.

Attributes

Name	Description
Index	'number'

Parents This element can have the following parents: <Pods> (see [page 86](#)).

Example <Pod Index='0' />

<Pods> Element

The <Pods> element contains the pods used by a defined probe.

Children This element can have the following children: <Pod> (see [page 85](#)).

Parents This element can have the following parents: <Probe> (see [page 87](#)).

Example

```
<Pods>
  <Pod Index='0' />
  <Pod Index='1' />
</Pods>
```

<Probe> Element

The <Probe> element describes a defined probe.

Attributes

Name	Description
Name	'string' (name of connector in device under test)
Type	'string' (name of probe)

Children This element can have the following children: <Pods> (see [page 86](#)), <Signals> (see [page 94](#)).

Parents This element can have the following parents: <DefinedProbes> (see [page 74](#)).

Example

```
<Probe Name='J1' Type='E5346A 34-ch Mictor single-ended probe'>
  <Pods>
    <Pod Index='0' />
    <Pod Index='1' />
  </Pods>
  <Signals>
    <Signal Name='ATD0' Pin='38' PinMapIndex='0' ClockChannel='F' />
    <Signal Name='ATD1' Pin='36' PinMapIndex='1' ClockChannel='F' />
    <Signal Name='ATD2' Pin='34' PinMapIndex='2' ClockChannel='F' />
    <Signal Name='ATD3' Pin='32' PinMapIndex='3' ClockChannel='F' />
    <Signal Name='ATD4' Pin='30' PinMapIndex='4' ClockChannel='F' />
    <Signal Name='ATD5' Pin='28' PinMapIndex='5' ClockChannel='F' />
    <Signal Name='ATD6' Pin='26' PinMapIndex='6' ClockChannel='F' />
    <Signal Name='ATD7' Pin='24' PinMapIndex='7' ClockChannel='F' />
    <Signal Name='ATD8' Pin='22' PinMapIndex='8' ClockChannel='F' />
    <Signal Name='ATD9' Pin='20' PinMapIndex='9' ClockChannel='F' />
    <Signal Name='ATD10' Pin='18' PinMapIndex='10' ClockChannel='F' />
    <Signal Name='ATD11' Pin='16' PinMapIndex='11' ClockChannel='F' />
    <Signal Name='ATD12' Pin='14' PinMapIndex='12' ClockChannel='F' />
    <Signal Name='ATD13' Pin='12' PinMapIndex='13' ClockChannel='F' />
    <Signal Name='ATD14' Pin='10' PinMapIndex='14' ClockChannel='F' />
    <Signal Name='ATCK' Pin='6' PinMapIndex='16' ClockChannel='T' />
  </Signals>
</Probe>
```

<Properties> Element

The <Properties> element contains setup information for the FPGA dynamic probe.

- Children** This element can have the following children: <ATC_II> (see [page 65](#)), <JTAG_Chain> (see [page 78](#)), <Devices> (see [page 77](#)).
- Parents** This element can have the following parents: "<Probe>" (in the online help).

When used in COM automation, this element is returned by the "QueryCommand method" (in the online help)'s GetAllSetup and GetProperties queries. You can also use this element string as an XMLCommand with the "DoCommands method" (in the online help) to configure the FPGA dynamic probe.

Example

```
<Properties>
  <ATC_II SelectedDevice='1' SelectedCore='1' CableType='0'
    ParallelCableType='0' ParallelCableSpeed='2'
    ParallelCablePort='0' USBCableSpeed='0' />
  <JTAG_Chain NumDevices='2' NumATC_II='2' />
  <Devices>
    <Device Name='Device 0' Type='0' NumCores='0' UserRegNum='0'
      Configurable='F' IRLength='8' CDCFilename=''
      FPGAFilename='' SelectedForUse='F'>
    <Cores />
  </Device>
  <Device Name='Device 1' Type='0' NumCores='2' UserRegNum='1'
    Configurable='T' IRLength='6' CDCFilename='C:\Documents
    and Settings\user\My Documents\Agilent Technologies\Logic
    Analyzer\Config Files\demo\Altera_demo_V8.cdc'
    FPGAFilename='C:\Documents and Settings\user\My
    Documents\Agilent Technologies\Logic Analyzer\Config
    Files\demo\Altera_demo_V8.bit' SelectedForUse='F'>
  <Cores>
    <Core Name='Core 0' Type='0' SelectedBank='0'
      SelectedSignal='-1' NumBanks='5' NumSignals='16'
      NumPins='9' StateMode='T' TDM_1X='F'
      ThresholdCode='92' TestBankAvailable='T'
      ClockPodIndex='0' SelectedForUse='T'
      CoreIsMaster='F' CoreCannotBeMaster='F'
      MinimumPeriod='-1' TestBankMode='2' Latency='4'>
    <Banks>
      ...
    </Banks>
    <PinMapping Attached='T' ModuleHandle='1'>
      ...
    </PinMapping>
  </Core>
  <Core Name='Core 1' Type='0' SelectedBank='0'
    SelectedSignal='-1' NumBanks='2' NumSignals='9'
    NumPins='9' StateMode='F' TDM_1X='T'
    ThresholdCode='92' TestBankAvailable='F'
```



```
        ClockPodIndex='2' SelectedForUse='T' CoreIsMaster='T'  
        CoreCannotBeMaster='F' MinimumPeriod='-1'  
        TestBankMode='0'>  
    <Banks>  
        ...  
    </Banks>  
    <PinMapping Attached='T' ModuleHandle='1'>  
        ...  
    </PinMapping>  
  </Core>  
</Cores>  
</Device>  
</Devices>  
</Properties>
```

<Signal> Element (under Bank)

The <Signal> element describes a signal within a bank.

Children This element can have the following children: <Labels> (see [page 81](#)).

Parents This element can have the following parents: <Signals> (see [page 92](#)).

Example

```
<Signal>
  <Labels>
    <Label Name='/s2mon/tid' Bit='0' />
  </Labels>
</Signal>
```

<Signal> Element (under Probe)

The <Signal> element describes a signal within a defined probe.

Attributes

Name	Description
ClockChannel	'F' (false) or 'T' (true)
Name	'string'
PinMapIndex	'number'

Parents This element can have the following parents: <Signals> (see [page 94](#)).

Example `<Signal Name='ATD0' Pin='38' PinMapIndex='0' ClockChannel='F' />`

<Signals> Element (under Bank)

The <Signals> element contains descriptions of signals within a bank.

Children This element can have the following children: <Signal> (see [page 90](#)).

Parents This element can have the following parents: <Bank> (see [page 66](#)).

Example

```
<Signals>
  <Signal>
    <Labels>
      <Label Name='/s2mon/tid' Bit='0' />
    </Labels>
  </Signal>
  <Signal>
    <Labels>
      <Label Name='/s2mon/tid' Bit='1' />
    </Labels>
  </Signal>
  <Signal>
    <Labels>
      <Label Name='/s2mon/tid' Bit='2' />
    </Labels>
  </Signal>
  <Signal>
    <Labels>
      <Label Name='/s2mon/tid' Bit='3' />
    </Labels>
  </Signal>
  <Signal>
    <Labels>
      <Label Name='/s2mon/tid' Bit='4' />
    </Labels>
  </Signal>
  <Signal>
    <Labels>
      <Label Name='/s2mon/tid' Bit='5' />
    </Labels>
  </Signal>
  <Signal>
    <Labels>
      <Label Name='/s2mon/tid' Bit='6' />
    </Labels>
  </Signal>
  <Signal>
    <Labels>
      <Label Name='/s2mon/tid' Bit='7' />
    </Labels>
  </Signal>
  <Signal>
    <Labels>
      <Label Name='/s2mon/lastackid' Bit='0' />
    </Labels>
  </Signal>
</Signals>
```

```
        <Label Name='/s2mon/lastackid' Bit='1' />
    </Labels>
</Signal>
<Signal>
    <Labels>
        <Label Name='/s2mon/lastackid' Bit='2' />
    </Labels>
</Signal>
<Signal>
    <Labels>
        <Label Name='/s2mon/lastackid' Bit='3' />
    </Labels>
</Signal>
<Signal>
    <Labels>
        <Label Name='/s2mon/lastackid' Bit='4' />
    </Labels>
</Signal>
<Signal>
    <Labels>
        <Label Name='/s2mon/lastackid' Bit='5' />
    </Labels>
</Signal>
<Signal>
    <Labels>
        <Label Name='/s2mon/lastackid' Bit='6' />
    </Labels>
</Signal>
    <Labels />
</Signal>
</Signals>
```

<Signals> Element (under Probe)

The <Signals> element contains the signals used by a defined probe.

Children This element can have the following children: <Signal> (see [page 91](#)).

Parents This element can have the following parents: <Probe> (see [page 87](#)).

Example

```
<Signals>
  <Signal Name='ATD0' Pin='38' PinMapIndex='0' ClockChannel='F' />
  <Signal Name='ATD1' Pin='36' PinMapIndex='1' ClockChannel='F' />
  <Signal Name='ATD2' Pin='34' PinMapIndex='2' ClockChannel='F' />
  <Signal Name='ATD3' Pin='32' PinMapIndex='3' ClockChannel='F' />
  <Signal Name='ATD4' Pin='30' PinMapIndex='4' ClockChannel='F' />
  <Signal Name='ATD5' Pin='28' PinMapIndex='5' ClockChannel='F' />
  <Signal Name='ATD6' Pin='26' PinMapIndex='6' ClockChannel='F' />
  <Signal Name='ATD7' Pin='24' PinMapIndex='7' ClockChannel='F' />
  <Signal Name='ATD8' Pin='22' PinMapIndex='8' ClockChannel='F' />
  <Signal Name='ATD9' Pin='20' PinMapIndex='9' ClockChannel='F' />
  <Signal Name='ATD10' Pin='18' PinMapIndex='10' ClockChannel='F' />
  <Signal Name='ATD11' Pin='16' PinMapIndex='11' ClockChannel='F' />
  <Signal Name='ATD12' Pin='14' PinMapIndex='12' ClockChannel='F' />
  <Signal Name='ATD13' Pin='12' PinMapIndex='13' ClockChannel='F' />
  <Signal Name='ATD14' Pin='10' PinMapIndex='14' ClockChannel='F' />
  <Signal Name='ATCK' Pin='6' PinMapIndex='16' ClockChannel='T' />
</Signals>
```

<SymbolInfo> Element

The <SymbolInfo> elements contain the module bus/signal symbol settings associated with a particular bank.

Attributes

Name	Description
ModuleHandle	'number'
SymbolSettings	'string'

Parents This element can have the following parents: <Bank> (see [page 66](#)).

Example

```
<SymbolInfo ModuleHandle='1' SymbolSettings='
  <Module>
    <BusSignalSetup>
      <BusSignals>
        <BusSignal Name='My Bus 1' />
        <Folder Name='Core 0 FPGA Probe'
          Comment='Created by FPGA Dynamic Probe-1'>
          <BusSignal Name='/s2mon/tid' />
          <BusSignal Name='/s2mon/s2mstate' />
        </Folder>
      </BusSignals>
      <NetlistImport />
    </BusSignalSetup>
    <Config TimeOfTrigger='1.110240661 Gs'
      CorrelatedTriggerTime='0 s'
      UserSkewTime='0 s' SystemTrigger='T' />
  </Module>
' />
```

See Also • "<Module> Element (under Configuration Setup)" (in the online help)

<TriggerInfo> Element

The <TriggerInfo> elements contain the module trigger settings associated with a particular bank.

Attributes

Name	Description
ModuleHandle	'number'
TriggerSettings	'string'

Parents This element can have the following parents: <Bank> (see [page 66](#)).

Example

```
<TriggerInfo ModuleHandle='1' TriggerSettings='
&lt;Module&gt;
  &lt;Trigger Mode=&apos;State&apos; Type=&apos;Normal&apos;&gt;
    &lt;StoreQual Mode=&apos;Custom&apos;&gt;
      &lt;Event ParensNeeded=&apos;F&apos;&gt;
        &lt;Anything/&gt;
      &lt;/Event&gt;
    &lt;/StoreQual&gt;
    &lt;Step Number=&apos;1&apos;&gt;
      &lt;If&gt;
        &lt;Event ParensNeeded=&apos;F&apos;&gt;
          &lt;BusSignal Name=&apos;/s2mon/tid&apos;
            Bit=&apos;All&apos; Operator=&apos;Equals&apos;
            Value=&apos;h3F&apos;/&gt;
          &lt;/Event&gt;
          &lt;Occurrence Value=&apos;1&apos;
            Mode=&apos;Eventual&apos;/&gt;
          &lt;Action&gt;
            &lt;TriggerAction Operator=&apos;Fill Memory&apos;&gt;
              &lt;StoreQual Mode=&apos;Custom&apos;&gt;
                &lt;Event ParensNeeded=&apos;F&apos;&gt;
                  &lt;DefaultStore/&gt;
                &lt;/Event&gt;
              &lt;/StoreQual&gt;
            &lt;/TriggerAction&gt;
          &lt;/Action&gt;
        &lt;/If&gt;
      &lt;/Step&gt;
    &lt;/Trigger&gt;
    &lt;Config TimeOfTrigger=&apos;1.110240661 Gs&apos;
      CorrelatedTriggerTime=&apos;0 s&apos;
      UserSkewTime=&apos;0 s&apos; SystemTrigger=&apos;T&apos;/&gt;
  &lt;/Module&gt;
' />
```

See Also • "<Module> Element (under Configuration Setup)" (in the online help)

<WindowInfo> Element

The <WindowInfo> elements contain the display window settings associated with a particular bank.

Attributes

Name	Description
WindowHandle	'number'
WindowSettings	'string'

Parents This element can have the following parents: <Bank> (see [page 66](#)).

Example

```
<WindowInfo WindowHandle='1' WindowSettings='
&lt;Setup&gt;
  &lt;Sampling PerDivision=&apos;5 ns&apos; Delay=&apos;0 s&apos;/&gt;
  &lt;BusSignals&gt;
    &lt;Clear/&gt;
    &lt;BusSignal Module=&apos;My 1682D-1&apos;
      Name=&apos;My Bus 1&apos; DefaultBase=&apos;Hex&apos;
      Color=&apos;hFFFFFF&apos; Height=&apos;30&apos;/&gt;
    &lt;BusSignal Module=&apos;My 1682D-1&apos;
      Name=&apos;/s2mon/tid&apos; DefaultBase=&apos;Hex&apos;
      Color=&apos;hFFFFFF&apos; Height=&apos;30&apos;/&gt;
    &lt;BusSignal Module=&apos;My 1682D-1&apos;
      Name=&apos;/s2mon/s2mstate&apos;
      DefaultBase=&apos;Hex&apos; Color=&apos;hFFFFFF&apos;
      Height=&apos;30&apos;/&gt;
    &lt;BusSignal Name=&apos;Time&apos; Color=&apos;hFFFFFF&apos;
      Height=&apos;30&apos;/&gt;
  &lt;/BusSignals&gt;
&lt;/Setup&gt;
' />
<WindowInfo WindowHandle='2' WindowSettings='
&lt;BusSignals&gt;
  &lt;Clear/&gt;
  &lt;BusSignal Module=&apos;My 1682D-1&apos;
    Name=&apos;Sample Number&apos; Color=&apos;hFFFFFF&apos;
    Alignment=&apos;Right&apos; Width=&apos;112&apos;/&gt;
  &lt;BusSignal Module=&apos;My 1682D-1&apos;
    Name=&apos;My Bus 1&apos; DefaultBase=&apos;Hex&apos;
    Color=&apos;hFFFFFF&apos; Alignment=&apos;Right&apos;
    Width=&apos;113&apos;/&gt;
  &lt;BusSignal Name=&apos;Time&apos; DefaultBase=&apos;Absolute&apos;
    Color=&apos;hFFFFFF&apos; Alignment=&apos;Right&apos;
    Width=&apos;152&apos;/&gt;
  &lt;BusSignal Module=&apos;My 1682D-1&apos;
    Name=&apos;/s2mon/tid&apos; DefaultBase=&apos;Hex&apos;
    Color=&apos;hFFFFFF&apos; Alignment=&apos;Right&apos;
    Width=&apos;113&apos;/&gt;
  &lt;BusSignal Module=&apos;My 1682D-1&apos;
    Name=&apos;/s2mon/s2mstate&apos; DefaultBase=&apos;Hex&apos;
    Color=&apos;hFFFFFF&apos; Alignment=&apos;Right&apos;
    Width=&apos;120&apos;/&gt;
&lt;/BusSignals&gt;
' />
```

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```
</BusSignals>  
' />
```

See Also • "<Window> Element (under Configuration Setup)" (in the online help)

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